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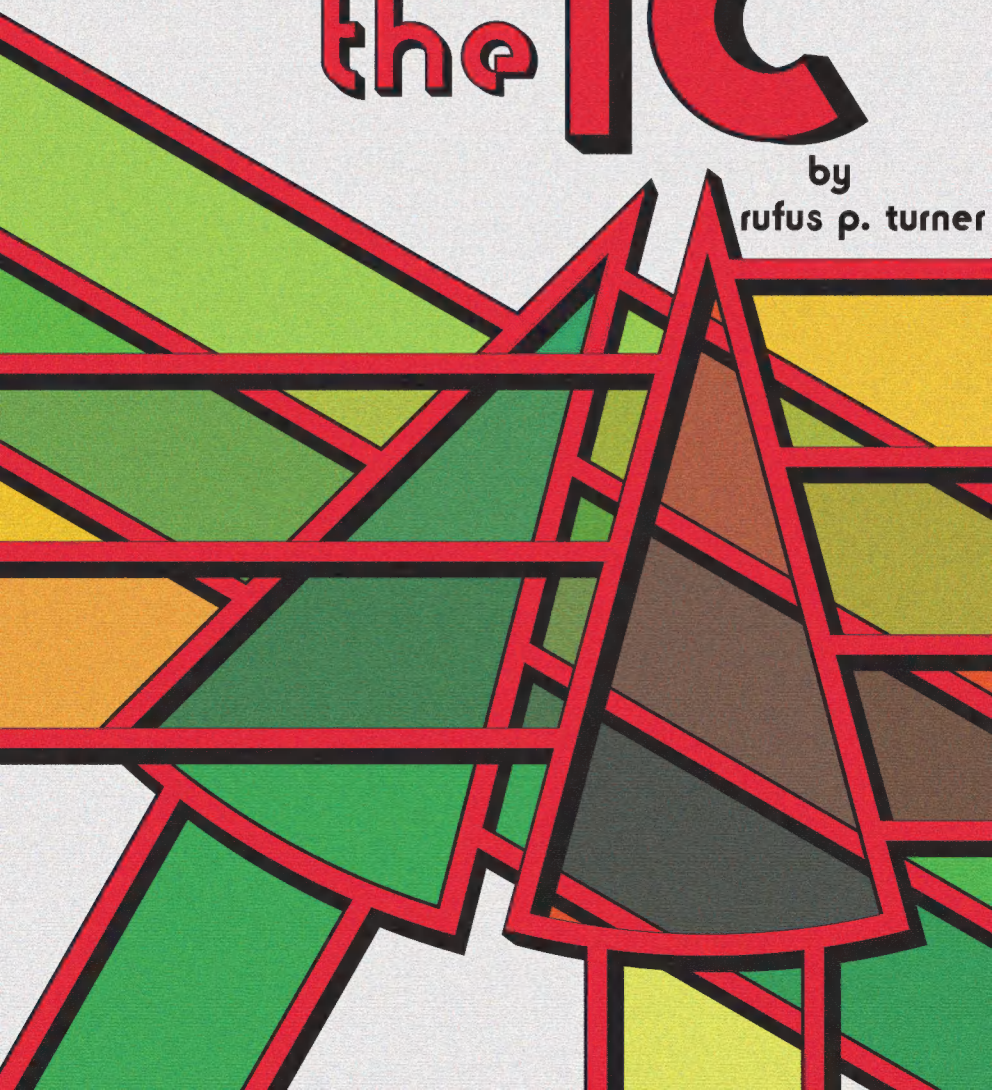
getting acquainted with the IC

by rufus p. turner



Getting Acquainted With the IC

by

Rufus P. Turner, PhD

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Preface

This book is addressed to those who wish to become familiar with the integrated circuit as quickly as possible and who prefer a "hands-on" approach. Our method is to have the reader test an IC for its various electrical characteristics, thus determining how it works. This approach has enjoyed success in the teaching of tube and transistor fundamentals.

Part 1 offers a brief introduction to the integrated circuit. This is the only theory discussed in the book; we assume that the reader is already familiar with diodes, transistors, rectifiers, and general semiconductor theory.

Part 2 is devoted entirely to practical tests and measurements. The cookbook-type presentation in this section aims to hold the IC novice on the preferred path and to keep him and his equipment out of trouble. The seasoned experimenter who just happens to be new to ICs should at least review our step-by-step procedure before he embarks upon a procedure of his own design.

Part 3 offers a series of simple applications of the IC used throughout Part 2. These will enable the reader to put the IC to work immediately.

RUFUS P. TURNER

Contents

PART 1

INTRODUCTION 11

1.1 Nature of the Integrated Circuit 11
1.2 The IC as a Unit 15
1.3 IC Symbols 16
1.4 Differential Amplifier in ICs 17
1.5 Operational-Amplifier IC 19
1.6 Economics of the Integrated Circuit 21
1.7 Precautions in Handling ICs 21
1.8 IC Used in This Book 22
1.9 Nature of Experiments in This Book 23

PART 2

EXPERIMENTS 27

Experiment 1. DC Operating Voltages 29
Experiment 2. Operating Current 30
Experiment 3. Output Offset Voltage 31
Experiment 4. Output Polarity 32
Experiment 5. Offset Null Adjustment 34
Experiment 6. Input Offset Voltage 37
Experiment 7. Input Offset Current 38
Experiment 8. Closed-Loop DC Voltage Gain 39
Experiment 9. Open-Loop AC Voltage Gain 42
Experiment 10. Closed-Loop AC Voltage Gain 43
Experiment 11. Open-Loop Frequency Response 44

PART 1

Introduction

Within a relatively short time, the integrated circuit (IC) has brought many improvements to electronics. Not only has it shortened the time needed to assemble a system, but it has also reduced the bulk, weight, and cost of the system. All electronics people must be on intimate terms with the IC.

This introduction offers a brief, elementary description of the IC. For a more comprehensive treatment, see *abc's of Integrated Circuits* by Rufus P. Turner (published by Howard W. Sams & Co., Inc., 1971).

1.1 NATURE OF THE INTEGRATED CIRCUIT

A semiconductor device, an integrated circuit is a silicon chip which contains microscopic components (diodes, transistors, resistors, and capacitors; as needed) and the interconnections ("wiring") between them. These are created inside the chip by electrochemical and photochemical processing of various areas of the chip. Integrated circuits run the gamut from simplicity to complexity. Thus, an IC may contain only a pair of diodes, it may be a multistage amplifier having several dozen components and all of their interconnections (and still be no larger than a small discrete transistor) or it may contain the complete heart of a digital timepiece or a microcomputer. Very often, the IC performs a function by itself, requiring only the application of dc voltages and the connection of input and output. In other in-

stances, only a few outboard components (e.g., resistors, capacitors, inductors, potentiometers, etc.) are needed.

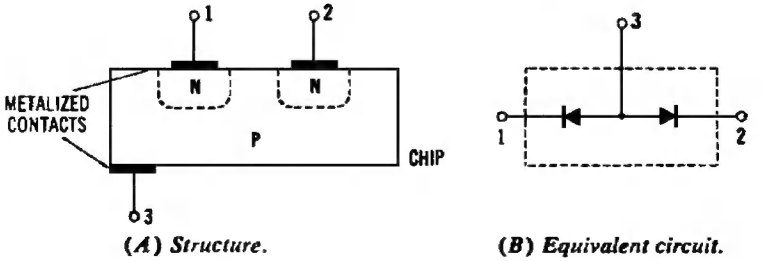
There are two general classes of integrated circuits: *linear ICs* include such analog devices as amplifiers, modulators, detectors, and so on; *digital ICs* include such switching devices as flip-flops, gates, adders, encoders, decoders, and so on.

Small size is not the only advantage of the IC; another is stability. Since all components in the IC are formed near each other in the chip, they are easily matched through controlled fabrication processes, and during operation they experience nearly the same temperature changes. Still another advantage is the labor saving afforded by the IC. Since all of the internal connections are provided in the simple plug-in integrated circuit, only external connections actually need to be wired.

This discussion will not explain how ICs are manufactured, for that is beyond the scope of this book. Instead, a simple description of IC structure will be given. Figs. 1-1 through 1-5 show this structure. These sketches do not show proportions accurately, since it would be difficult to preserve exact scales and still keep the various parts of the IC visible to the reader, but the sketches are sufficiently true for purposes of illustration.

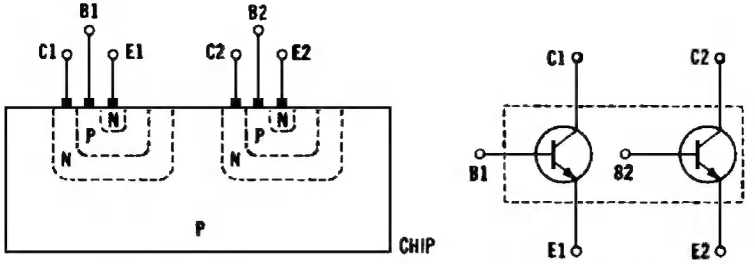
Fig. 1-1 shows a dual-diode (common-anode) IC. In Fig. 1-1A, two n regions have been diffused into a p-type chip to provide the pn junctions of the diodes. A thin spot of metal has been deposited on each n region and on the chip to provide contacts, and attached to these contacts are leads 1, 2, and 3. Fig. 1-1B shows the equivalent circuit.

Fig. 1-2 shows an IC containing two matched npn transistors. Here (Fig. 1-2A), the chip is p-type silicon into which n and p regions have been diffused for the emitters (E1, E2), bases (B1, B2), and collectors (C1, C2) of the transistors. A thin spot of metal deposited



(A) Structure. *(B) Equivalent circuit.*

Fig. 1-1. Matched-diode integrated circuit.

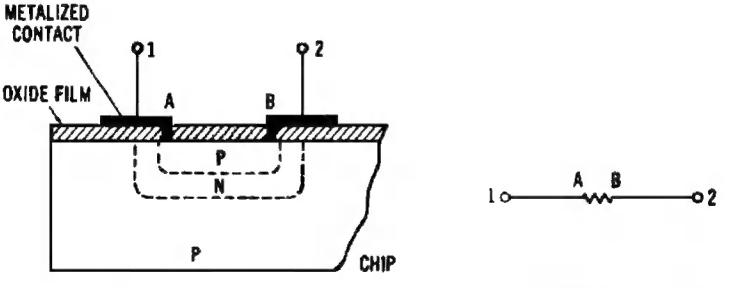


(A) Structure. *(B) Equivalent circuit.*

Fig. 1-2. Matched-transistor integrated circuit.

on each n region and on each p region provides contact, and attached to these contacts are leads C1, E1, and B1 for the first transistor; and C2, B2, and E2 for the second transistor. Fig. 1-2B shows the equivalent circuit.

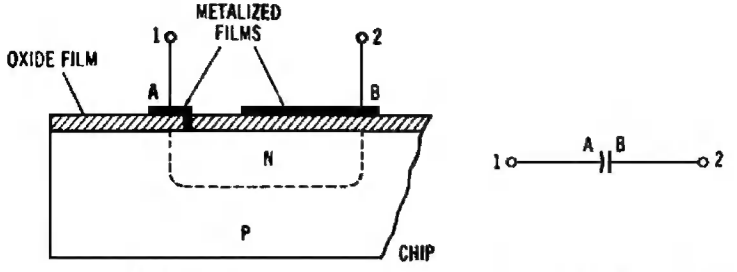
Fig. 1-3 shows how a resistor is formed in an IC. In Fig. 1-3A, the resistive element is the p region; a desired resistance value is obtained by suitably processing this region. An n layer isolates this resistor from the p-type chip. A thin oxide layer has been grown on the surface of the chip for protection, and this layer is penetrated through holes at *A* and *B* by thin deposits of metal which contact the ends of the integrated resistor. Leads 1 and 2 are connected to these contacts.



(A) Structure. *(B) Equivalent circuit.*

Fig. 1-3. Integrated resistor.

Fig. 1-4 shows how a capacitor is formed in an IC. In Fig. 1-4A, an n region has been processed into the p-type chip, and a thin oxide film then has been grown on the surface of the chip. The n region constitutes one plate of the capacitor, and the oxide film is the dielectric. A thin metallic film (*B*) deposited on the oxide film is the other plate of the capacitor. A thin metallic spot (*A*) has been deposited on

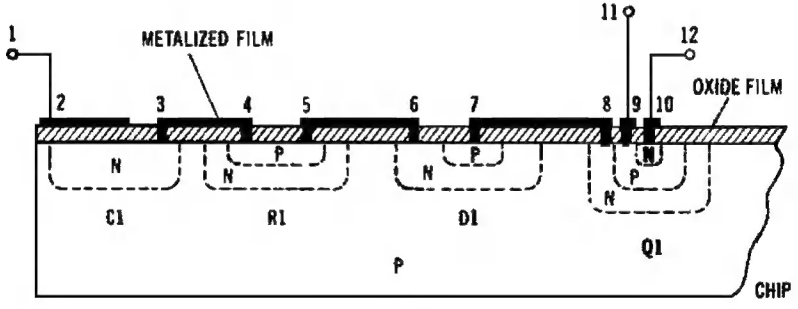


(A) Structure. *(B) Equivalent circuit.*

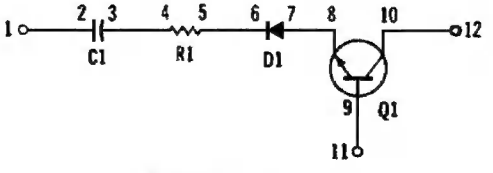
Fig. 1-4. Integrated capacitor.

the film, which it penetrates through a hole to contact one end of the n region. Leads 1 and 2 are attached to these film-type contacts. The area of plate *B* is chosen for a desired capacitance (for a given oxide-film thickness, the greater the area the higher the capacitance).

Integrated diodes, transistors, resistors, and capacitors—such as those in Figs. 1-1 through 1-4—may be combined in a number of ways to build into the chip any desired electronic device employing those components. Fig. 1-5, for example, shows how a single capacitor, resistor, diode, and transistor may be integrated into a chip to-



(A) Structure.



(B) Equivalent circuit.

Fig. 1-5. Example of complete integrated circuit.

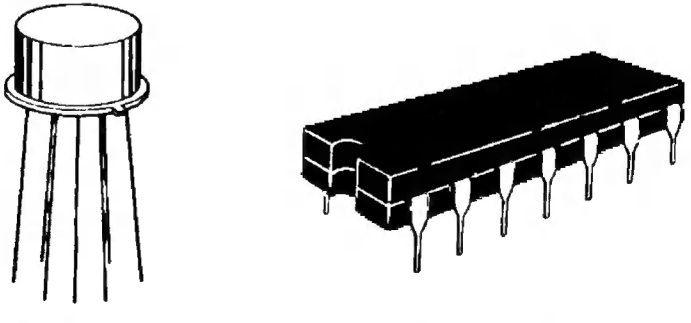
gether with all interconnections. While this is not necessarily a functional circuit, it gives as clear an illustration of the structure as is possible in two dimensions. Fig. 1-5A shows the cross section of the integrated series circuit of capacitor C1, resistor R1, diode D1, and npn transistor Q1. Fig. 1-5B gives the equivalent circuit. The components in Fig. 1-5A may readily be identified separately from Figs. 1-1 through 1-4. Note how the components are interconnected: The metal film between points 3 and 4 connects the capacitor to the resistor, the film between 5 and 6 connects the resistor to the diode, and the film between 7 and 8 connects the diode to the transistor. External leads 1, 11, and 12 are connected to the film at points 2, 9, and 10, respectively.

1.2 THE IC AS A UNIT

An integrated circuit is equipped with leads or lugs, so that it may be plugged into a small socket or soldered to points on a foundation. such as a printed circuit board. Several different IC packages are obtainable. Two of the most common of these are shown in Fig. 1-6.

Fig. 1-6A shows the TO-5 style of metal case, which is very familiar as a transistor package. The IC shown has eight leads, but 10- and 12-lead ICs also are available in TO-5 cans. The diameter of the TO-5 can is a little more than ¼ inch, and the leads are ½-inch long.

Fig. 1-6B shows the dual–in-line package (DIP). This is a molded plastic housing having terminal pins (seven or eight) along each long edge. The 14-pin package is approximately ¾-inch long and ¼-inch wide. Similar rectangular packages also are supplied: *mini-DIP* (eight leads) and *flat pack* (10 leads).



(A) TO-5 case. *(B) Dual–in-line case.*

Fig. 1-6: Common IC packages.

1.3 IC SYMBOLS

Fig. 1-7 shows circuit symbols for a representative sampling of integrated circuits, according to function. Figs. 1-7A and 1-7B represent linear ICs. Figs. 1-7D through 1-7G and 1-7I through 1-7K represent digital ICs. Figs. 1-7C and 1-7H can be used to represent either linear or digital applications.

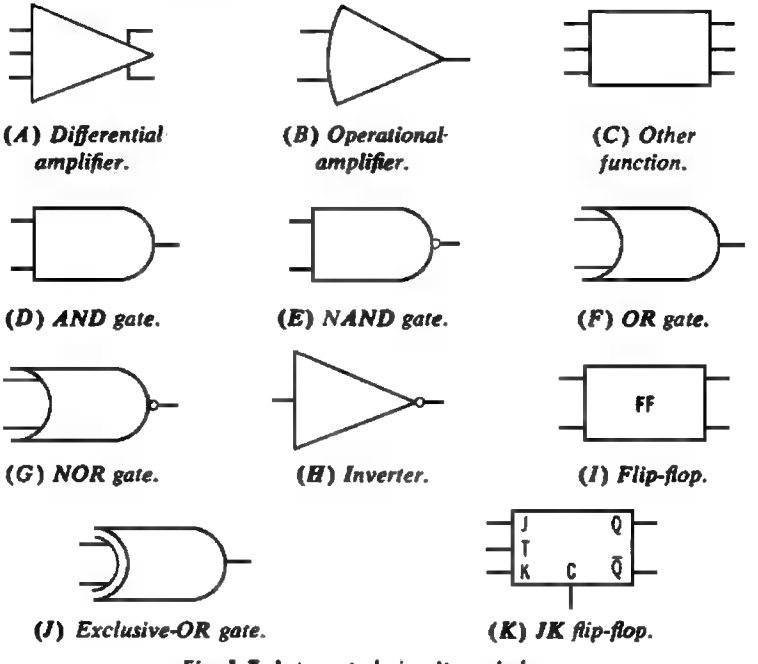


Fig. 1-7. Integrated-circuit symbols.

In each of these symbols, the convention of input terminals on the left and output terminals on the right is observed. The symbol in Fig. 1-7C can represent any IC (such as a voltage regulator, multiple transistors, etc.) for which there is no other specific symbol The block must be labeled with the IC type number, and each lead must be appropriately numbered to correspond to the IC base numbering. It should be mentioned here that some publications do not use the specific functional symbols, but represent all ICs with a simple triangle similar to Fig. 1-7A.

While the basic symbols in Fig. 1-7 show only input and output signal connections, all connections must be shown in a wiring diagram. Such a complete presentation is illustrated in Fig. 1-8. Here,

a CA3002 integrated circuit is shown with all ten of its leads. Although the numbering corresponds to that of the leads of the actual

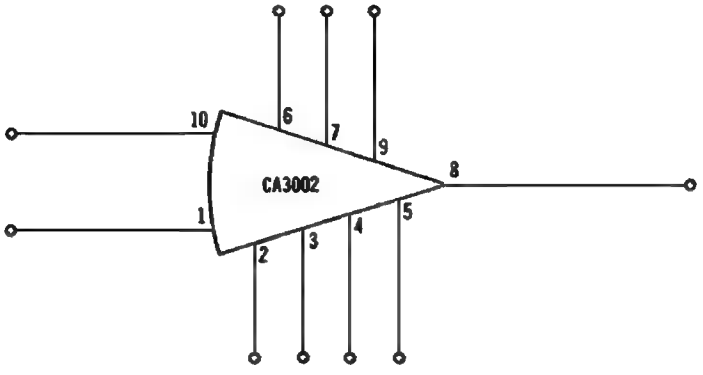


Fig. 1-8. Labeled IC symbol.

IC, it is not always shown consecutively in a schematic. Instead, the *correctly numbered* leads (except input and output) are drawn wherever clarity will be ensured in the schematic.

1.4 DIFFERENTIAL AMPLIFIER IN ICs

A great many ICs employ a differential amplifier in the input stage, and some have differential amplifiers in other direct-coupled stages, as well. The differential amplifier is used because it is inherently one that reduces drift caused by shifts in current and temperature and the aging of components, and it does this without inadvertently cancelling out the input signal. Some ICs, such as the Type CA3000, consist only of a differential amplifier.

Fig. 1-9 shows a bare-bones version of the differential amplifier, offered here for discussion. The two transistors (Q1, Q2) and the two collector resistors (R_{C1}, R_{C2}) are closely matched, and collector bias voltage V_{CC} equals emitter bias voltage V_{EE}. Because of this matching and the bridge-like symmetry of the circuit, any drift in the left leg of the circuit is cancelled by an equal drift in the right leg. If a separate signal is applied to each input, the output will be proportional to the difference between the two, and this accounts for the name differential amplifier. If, however, the same signal is applied to both inputs, ideally it will be cancelled and the output will be zero. This brings up several terms: Performance with the signal applied simultaneously to

both inputs is called *common-mode operation*. If the circuit is really balanced, it will transmit no signal in this condition, and the *common-mode gain* is zero. Conversely, the *common-mode rejection* is infinite. If a signal is applied to one input only, with the other input grounded, the signal will be amplified normally.

In a good differential amplifier, the common-mode rejection must be high without degrading normal gain of the amplifier. This is accomplished by making resistance R_{EE} very high. But when R_{EE} is increased, voltage V_{EE} also must be increased. High V_{EE} in combination with high R_{EE} constitutes a constant-current supply, which shows that the ideal situation is to drive the differential amplifier from a controlled constant-current source. A far more efficient method than high voltage plus high resistance is to use a constant-current device with a low voltage. The normal value of V_{EE} (equal to V_{CC}) then may be used. This arrangement is shown in Fig. 1-10, where the constant-current conduction characteristic of common-emitter transistor Q3 is exploited. The combination of this transistor, resistors R1 and R2, and diodes D1 and D2 constitutes the *constant-current sink*. (In some ICs, the sink is somewhat more elaborate than this example.)

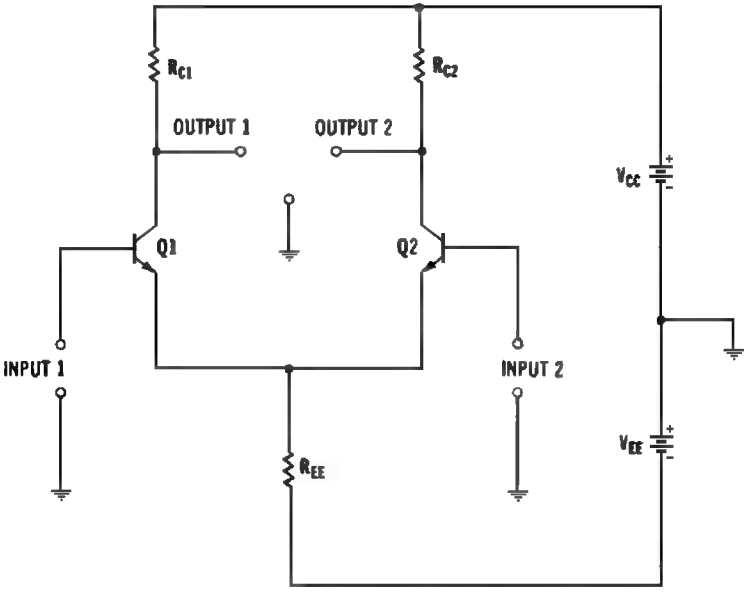


Fig. 1-9. Basic differential amplifier

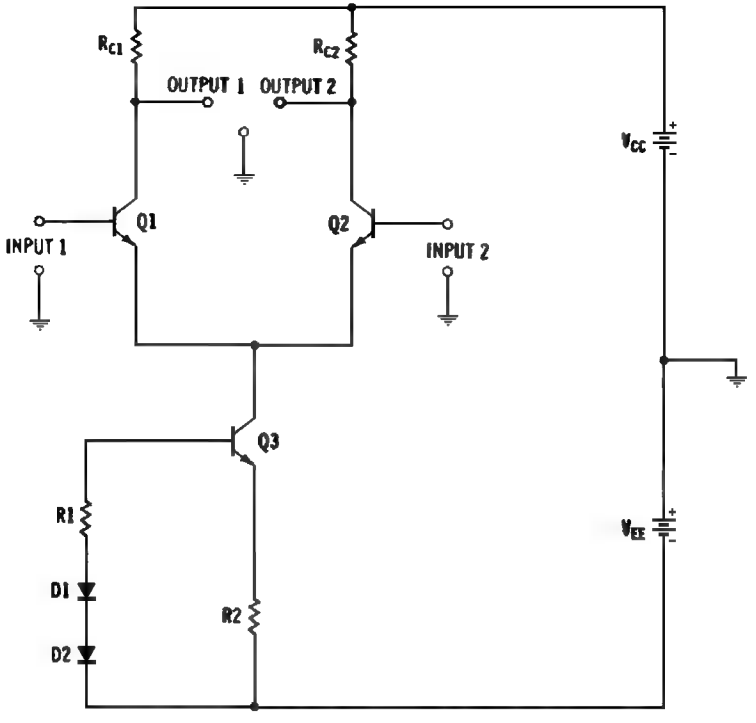


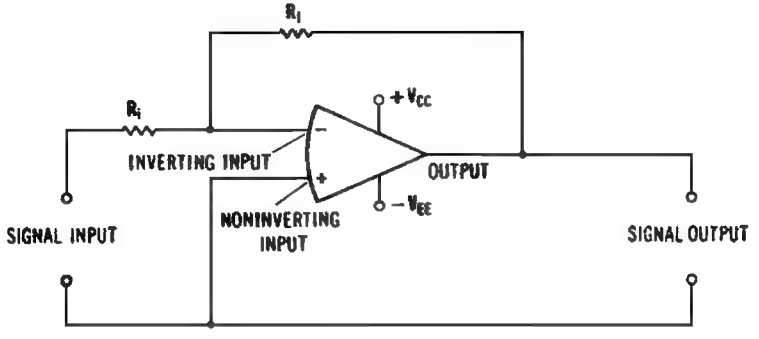
Fig. 1-10. Differential amplifier with current sink.

1.5 OPERATIONAL-AMPLIFIER IC

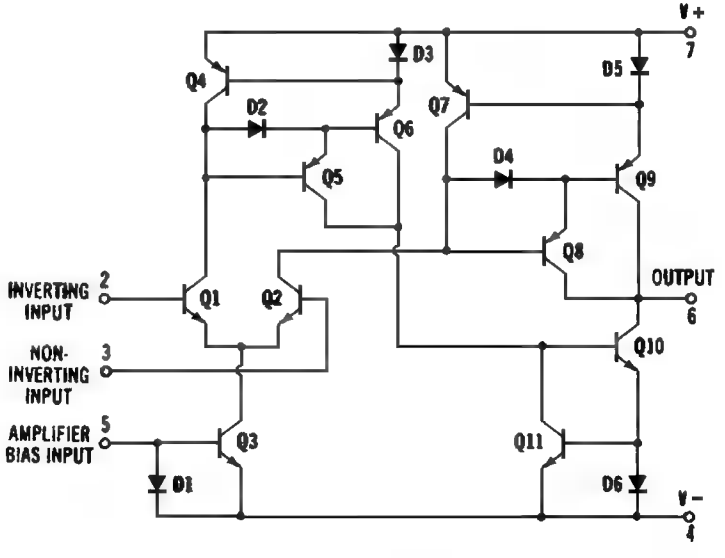
A large number of ICs are *operational amplifiers* (*op amps*). The typical operational amplifier has differential input and single-ended output. Its input impedance is high, and its output impedance is low. The open-loop voltage gain of the op amp is extremely high, so that large amounts of external feedback may be employed without reducing the gain below a useful level. This allows the transmission characteristic of the amplifier to be shaped by the feedback network. Extremely high input impedance is achieved in some op amps through the use of field-effect transistors (JFETs or MOSFETs) in the input differential-amplifier stage.

Fig. 1-11A shows a typical op-amp setup. The two inputs of the device are termed *inverting* and *noninverting*. This means that when a signal is applied to the noninverting input, the signal emerges in the same phase at the output, but when the signal is applied to the inverting input, the output signal has the opposite phase. External

resistor R_f is connected from the output to the inverting input (−) and therefore provides a negative feedback path. Connected instead to the noninverting input (+), it would introduce positive feedback.



(A) Typical op-amp setup.



(B) Internal circuit of representative op amp.

Fig. 1-11. Operational-amplifier IC.

The closed-loop voltage gain in Fig. 1-11A is determined by the ratio of feedback resistance (R_f) to amplifier input resistance (R_i): $A_v = R_f/R_i$. Fig. 1-11B shows the internal circuit of a representative op amp (RCA Type CA3080)

For an extensive treatment of the operational amplifier, see *IC Op-Amp Cookbook* by Walter G. Jung (published by Howard W. Sams & Co., Inc., 1974).

1.6 ECONOMICS OF THE INTEGRATED CIRCUIT

Integrated circuits provide significant size, weight, and labor-saving advantages. In addition, they offer a substantial cost bonus in the assembly of larger electronic systems. A typical example is an operational amplifier selling at the time of this writing for 80 cents retail. This IC contains 20 transistors, 11 resistors, and 1 capacitor—components that would cost about $33 in the retail market and would still need to be wired up.

1.7 PRECAUTIONS IN HANDLING ICs

Before starting the tests and experiments in Part 2 of this book, read closely the following tips on handling integrated circuits. Proper handling will not only protect the IC, but will also enhance the progress of the experiment.

A. Mechanical Shock. Like other semiconductor devices, the IC is a surprisingly rugged component. Nevertheless, it should not be abused by dropping, hammering, squeezing, pulling, and so on. Treat it as if it were a more delicate component.

B. Input Protection. When the IC contains an *unprotected* MOSFET input stage, keep the short-circuiting device in place until the IC is completely installed. A gate-protected IC, such as Type CA3140, has self-contained protective zener diodes and does not require this special handling.

C. Installation. Most ICs are tiny devices having a number of leads or pins spaced closely together. This demands considerable manual dexterity in handling the IC and in making connections to it. Be sure the leads do not touch each other; use tweezers to separate them. In a test setup, it is better to plug the IC into a socket or breadboard than to connect it with clip leads. Use the full length of IC leads; do not clip them unless you are sure you can straighten and align the shortened leads. Check all wiring in a setup carefully, and install the IC *last*. When the test is over, remove the IC first.

D. Soldering. Heat-sink the leads of an IC before soldering. If it is impracticable to use a heat sink, then solder rapidly and blow cool air on the joint immediately afterward.

E. Power-Supply Polarity. Carefully observe the polarities of the dc supplies. Reversing positive and negative may damage the IC.

F. Sequence in Energizing. Apply the dc operating voltage(s) *after* the IC has been installed in a setup. When the test is finished, disconnect the dc *before* the IC is removed. When a dual dc supply is used, open and close both dc circuits simultaneously. Apply the signal *after* the power is on.

G. Maximum Ratings. Keep all signal and bias voltages and currents and the power dissipation within the maximum limits specified by the IC manufacturer.

H. Input/Output Isolation. Keep the signal input and output circuits isolated from each other; otherwise, the high gain of the IC may encourage undesired output-to-input coupling.

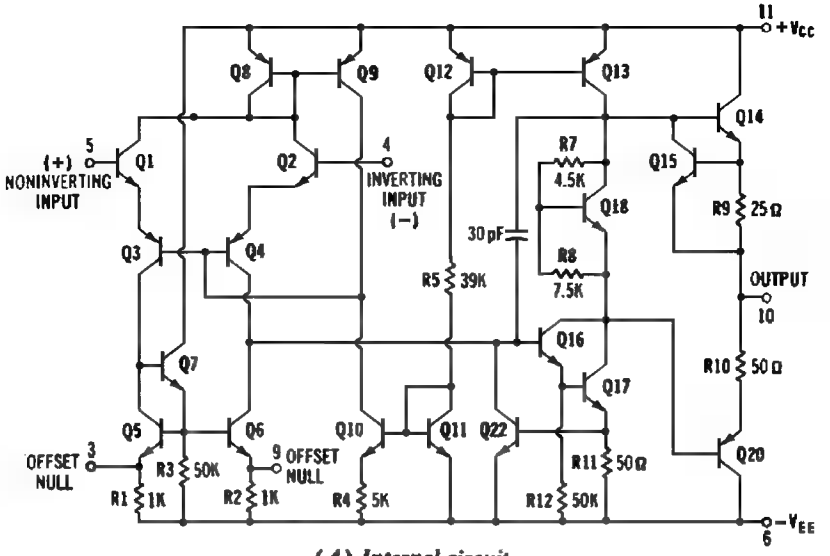
I. Temperature. Like other semiconductor devices, the IC has some sensitivity to temperature. The operating temperature of the device therefore must be kept within the limits specified by the manufacturer. Unless a temperature-effect test is under way, keep the IC at room temperature; in any test setup, keep the IC away from hot components. During a temperature test, hold the temperature of the IC at each level only so long as is needed for the electrical characteristic under study to stabilize at that level.

J. Fields. Keep the IC out of intense magnetic and electric fields both af and rf.

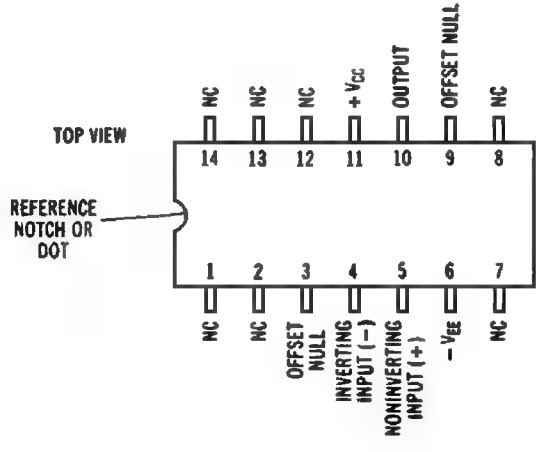
1.8 IC USED IN THIS BOOK

The Type 741 integrated circuit is used in the experiments in this book. This device is an inexpensive, general-purpose op amp that is widely available on a single-unit retail basis. The internal circuit of the 741 is shown in Fig. 1-12A, and a top view of the 14-contact, dual–in-line package (DIP) is shown in Fig. 1-12B. It is worth noting here that the 741 is obtainable also in a TO-5 can (8 leads), a flat pack (10 leads), and a mini-DIP package (8 leads). However, the lead numbering in Fig. 1-12 pertains only to the DIP package.

The 741 has some important advantages. Among these are: (A) its output is short-circuit protected, (B) this IC is internally compensated (by means of a 30-pF integrated capacitor between transistors Q16 and Q18 in Fig. 1-12A), (C) provision is made for offset null (terminals 3 and 9 in Fig. 1-12), and (D) the 741 is free from latch-up (the condition in which the input stage is held in saturation by feedback which has changed from negative to positive).



(A) Internal circuit.



(B) DIP package

Fig. 1-12. Type 741 integrated circuit.

1.9 NATURE OF EXPERIMENTS IN THIS BOOK

The purpose of the experiments in Part 2 is to test the electrical characteristics of the IC and in this way to obtain a hands-on familiarity with the device. The 741 integrated circuit is employed through-

out. A minimum of equipment is required and need not be of expensive laboratory grade. Required apparatus is listed at the head of each experiment. A positive dc supply and a negative dc supply are needed. These may be batteries, but greater flexibility will be obtained with power-line–operated variable-voltage units.

Except where noted otherwise, the layout of the test circuit is not critical, and the reader therefore is free to indulge his preferences. In setting up a test, most experimenters, however, will probably favor one of the modern plug-in breadboards, since these require no soldering and they afford speedy building up and tearing down of a test circuit. Also, they allow components to be changed easily.

The experiments may be performed either sequentially or randomly, depending upon the reader's need for information about the IC. We recommend that the beginner who is meeting the IC for the first time perform the experiments in the order in which they are arranged in Part 2.

PART 2

Experiments

The following pointers are offered for the guidance of the experimenter. Please read them carefully before embarking upon the experiments. In addition to containing material essential to the success of experiments, they offer certain information which will not be repeated in individual experiments.

1. Sequence. The experiments are arranged in an order which uncovers various information concerning the IC, starting with the simplest characteristics and proceeding through more sophisticated ones. The reader is not compelled to follow this sequence, but the newcomer to ICs doubtless will find it helpful to do so.

2. Step-by-Step Procedure. The cookbook-type directions in this part were developed to insure success of the experiment and to minimize the chance of damaging the apparatus. The reader is strongly urged to follow the procedures as they are given.

3. Integrated Circuit. The same type of IC is used in each experiment: the Type 741 operational amplifier. Use a *new* IC. Surplus ones sometimes are rejects having high offset which will ruin some of the experiments. See Section 1.7 in Part 1 for precautions in working with ICs.

4. Terminal Labeling. Numbering of the IC terminals in the schematics is not in the sequence in which the terminals of the actual unit are arranged (Fig. 1-12, Part 1), but has been chosen for clarity of the diagram. Unused terminals are omitted from the drawing.

5. DC Supply. A split dc supply is shown in each experiment. For drafting convenience, batteries are shown, and their use is permissible. However, low-ripple, power-line–operated supplies also can be

used and are preferred in most instances. Several excellent, small-sized units are available which supply separate, variable positive and negative outputs. In the experiments, the voltages must be set to the levels shown in the schematics.

6. DC Test Signal. A dc input signal is required in a number of experiments. This signal is supplied by a 1½-volt cell. A *fresh* size-C flashlight cell is satisfactory for this purpose.

7. AC Test Signal. See *10. Signal Generators.*

8. Meters. Service-type meters are satisfactory. Voltmeters for dc should be 20,000 ohms per volt or higher. (Use an electronic voltmeter—vacuum-tube, transistor, or FET—where specified.) Voltmeters for ac should be of the electronic type. Millivoltmeters for dc also must be electronic, as the nonelectronic type has too low an internal resistance. An accuracy of ±2% of full scale is satisfactory for the nonelectronic meters; ±5% of full scale is satisfactory for the electronic meters.

9. Instrument Switching. In some circuits (such as Fig. 2-16), a single meter is switched alternately between input and output. In other circuits (such as Fig. 2-17), separate input and output meters are shown. Where separate meters appear, the circuit is susceptible to oscillation arising from feedback through switch wiring, so the use of a meter switch is discouraged.

10. Signal Generators. Most required ac signals are sine waves or square waves in the audio-frequency range. Only a few experiments call for a 100- or 200-kHz signal. The maximum frequency in any experiment is 1 MHz. A reliable sine/square-wave audio generator may be used for the lower frequencies (most such instruments tune up to 200 kHz), and an rf signal generator having up to 1 volt rms output may be used for the 1-MHz signal. Generators used in the experiments should have low output impedance (500 ohms is good; 50 ohms is better). A good function generator will satisfy all requirements: frequency, waveform, and impedance.

11. Oscilloscope. Some experiments—specifically Nos. 9, 11, 15, 20, and 22—call for an oscilloscope having a voltage-calibrated vertical axis; and one experiment (No. 23) calls for one with a time-calibrated horizontal axis, as well. In any other instance, a basic oscilloscope will suffice.

12. Leads. Keep all leads as short as practicable, and run them as directly as possible even when a plug-in breadboard is used.

13. Resistors. All fixed resistors are 5% or 10% ¼-watt composition units.

14. Capacitors. Capacitors are nonelectrolytic (minimum rating, 50 V). Ceramics and Mylars are suitable.

15. Potentiometers. Potentiometers are composition type, except where noted ("ww") as wirewound

EXPERIMENT 1. DC OPERATING VOLTAGES

Required Equipment (Fig. 2-1)

1 741 integrated circuit
1 dc voltmeter (M1)
1 dpst switch (S1-S2)
1 +12 V dc supply (V_{CC})
1 −12 V dc supply (V_{EE})

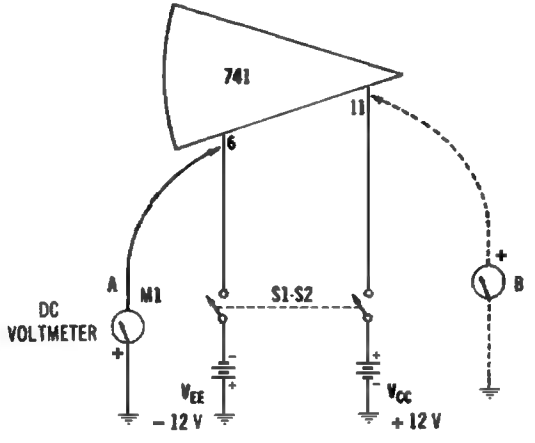


Fig. 2-1. Dc operating voltages.

Test Procedure

1. With switch S1-S2 open, set up the test circuit as shown in Fig. 2-1.
2. Close switch S1-S2.
3. With voltmeter M1 in position A and with its positive lead grounded, check the voltage *at* terminal 6 of the IC. Record. This is the negative voltage of the IC.
4. With voltmeter M1 in position B and with its negative lead grounded, check the voltage *at* terminal 11 of the IC. Record. This is the positive voltage of the IC.

(In all measurements of operating voltage in IC circuits, check the voltage in the above manner, i.e., *at* the IC contact. When the voltage

is measured at the dc supply or at an input terminal on the chassis, error can be caused by series outboard components or faulty leads.

Sample Results

$V_{CC} = +12$ V
$V_{EE} = -12$ V

EXPERIMENT 2. OPERATING CURRENT

Required Equipment (Fig. 2-2)

1 741 integrated circuit
1 0–10 dc milliammeter (M1)
1 dpst switch (S1-S2)
1 10K resistor (R1)
1 100K resistor (R2)
1 +15 V variable dc supply (V_{CC})
1 −15 V variable dc supply (V_{EE})

Test Procedure

1. With switch S1-S2 open, set up the test circuit as shown in Fig. 2-2.

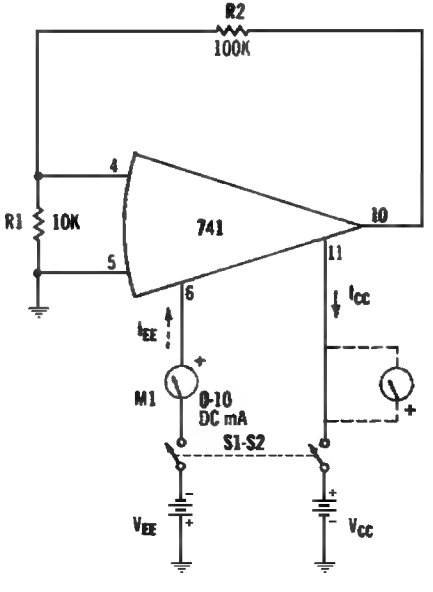


Fig. 2-2. Operating current.

Table 2-1. Sample Results, Operating Current

Supply Voltage	I_{CC}	I_{EE}
±15 V	2.2 mA	2.2 mA
±12 V	1.9 mA	1.9 mA
±9 V	1.5 mA	1.5 mA
±6 V	1.0 mA	1.0 mA

2. Set both dc supplies to zero.
3. Insert milliammeter M1 into the lead between negative supply V_{EE} and terminal 6 of the IC. *Be careful of meter polarity.*
4. Set both supplies to 6 V. Read the corresponding current value and record it under I_{EE} (see column 3 in Table 2-1).
5. Repeat with both supplies set successively to 9 V, 12 V, and 15 V. At each voltage step, read the corresponding current, and record it in the I_{EE} column.
6. Return both supply voltages to zero, and open switch S1-S2.
7. Remove milliammeter M1 from the V_{EE} lead and reconnect it in the lead between positive supply V_{CC} and terminal 11 of the IC (see dashed symbol in Fig. 2-2). Again, be careful of meter polarity. Restore the lead from negative supply V_{EE} to terminal 6 of the IC.
8. Set both supplies to 6 V. Read the corresponding current, and record it under I_{CC} (see column 2 in Table 2-1).
9. Repeat with both supplies set successively to 9 V, 12 V, and 15 V. At each voltage step, read the corresponding current, and record it in the I_{CC} column.

Sample Results

See Table 2-1.

EXPERIMENT 3. OUTPUT OFFSET VOLTAGE

Required Equipment (Fig. 2-3)

1 741 integrated circuit
1 electronic dc voltmeter/millivoltmeter (M1)
1 dpst switch (S1-S2)
1 10K resistor (R1)
1 100K resistor (R2)
1 +12 V dc supply (V_{CC})
1 −12 V dc supply (V_{EE})

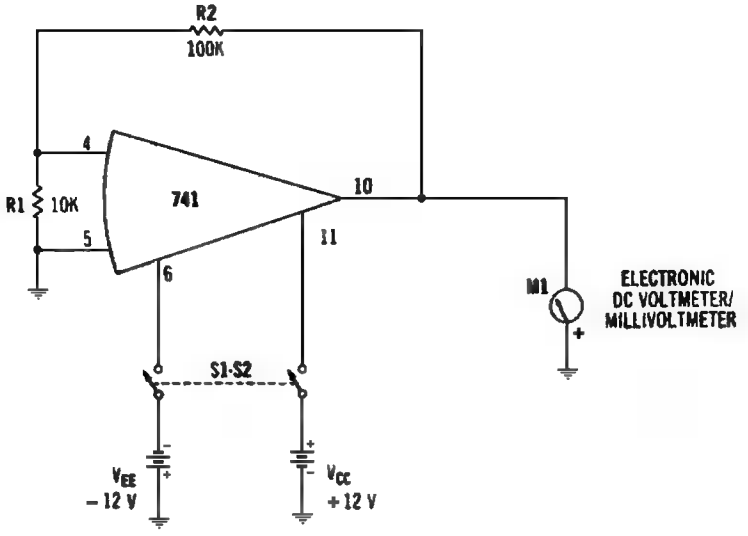


Fig. 2-3. Output offset voltage.

Test Procedure

1. With switch S1-S2 open, set up the test circuit as shown in Fig. 2-3.
2. Close switch S1-S2.
3. Note the deflection of meter M1 and the polarity of the offset voltage. (If the meter deflects downward, reverse its polarity. The offset voltage can be positive or negative, depending on the type of unbalance inside the IC.)

Sample Results

V_{offset} = 10 mV

EXPERIMENT 4. OUTPUT POLARITY

Required Equipment (Figs. 2-4 and 2-5)

1 741 integrated circuit
1 dc voltmeter (M1)
1 spst switch (S1)
1 dpst switch (S2-S3)
1 10K wirewound potentiometer (R1)
1 10K resistor (R2)
1 100K resistor (R3)
1 +12 V dc supply (V_{CC})

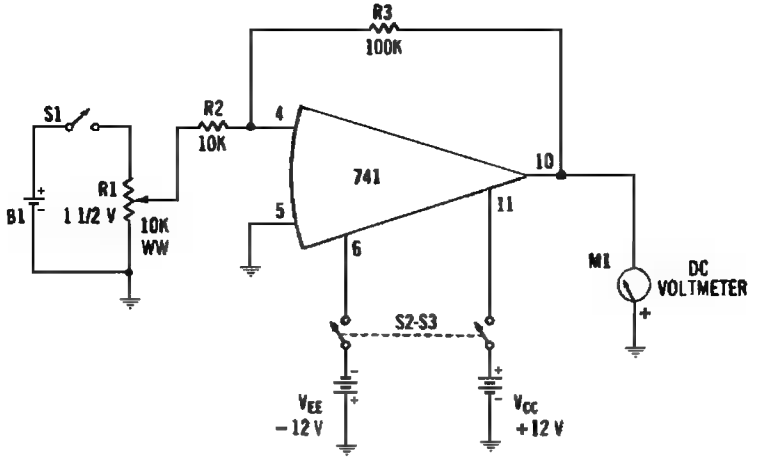


Fig. 2-4. Output polarity (step 1).

1 −12 V dc supply (V_{EE})
1 1½ V size-C cell (B1)

Test Procedure

Step 1

1. With switches S1 and S2-S3 open and with potentiometer R1 set to zero, set up the test circuit as shown in Fig. 2-4. Watch the meter polarity.
2. Close switch S2-S3

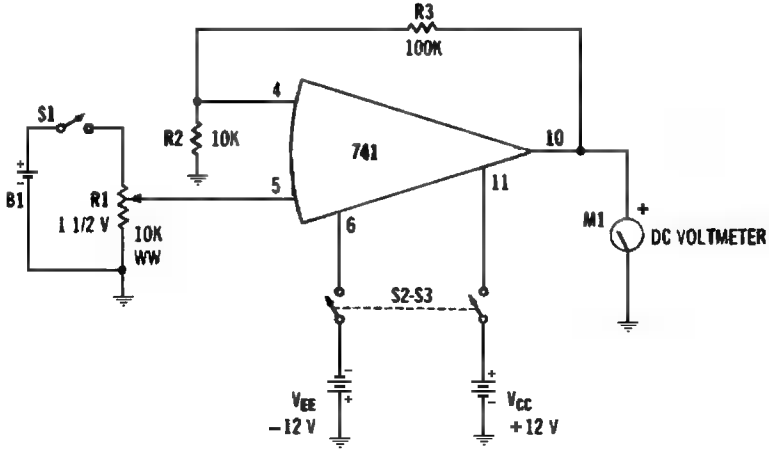


Fig. 2-5. Output polarity (step 2).

3. Close switch S1 and slowly increase the setting of potentiometer R1. This applies a positive signal to the inverting input of the IC.
4. Note the negative deflection of voltmeter M1.

Step 2

1. With switches S1 and S2-S3 open and with potentiometer R1 set to zero, set up the test circuit as shown in Fig. 2-5. Watch the meter polarity.
2. Close switch S2-S3.
3. Close switch S1, and slowly increase the setting of potentiometer R1. This applies a positive signal to the noninverting input of the IC.
4. Note the positive deflection of voltmeter M1

Sample Results

In Step 1, a positive signal applied to the inverting input (terminal 4 of the IC) gives a negative output signal. In Step 2, the same positive signal applied to the noninverting input (terminal 5 of the IC) gives a positive output signal.

EXPERIMENT 5. OFFSET NULL ADJUSTMENT

Required Equipment

This experiment consists of three steps, each requiring a different test circuit.

Step 1 (*Fig. 2-6*)

1 741 integrated circuit
1 dc voltmeter/millivoltmeter (M1)
2 dpst switches (S1-S2, S3-S4)
1 10K resistor (R1)
1 100K resistor (R3)
1 10K wirewound potentiometer (R2)
1 +12 V dc supply (V_{CC})
1 −12 V dc supply (V_{EE})

Step 2 (*Fig. 2-7*)

1 741 integrated circuit
1 electronic dc millivoltmeter (M1)
1 dc voltmeter (M2)
1 spst switch (S1)

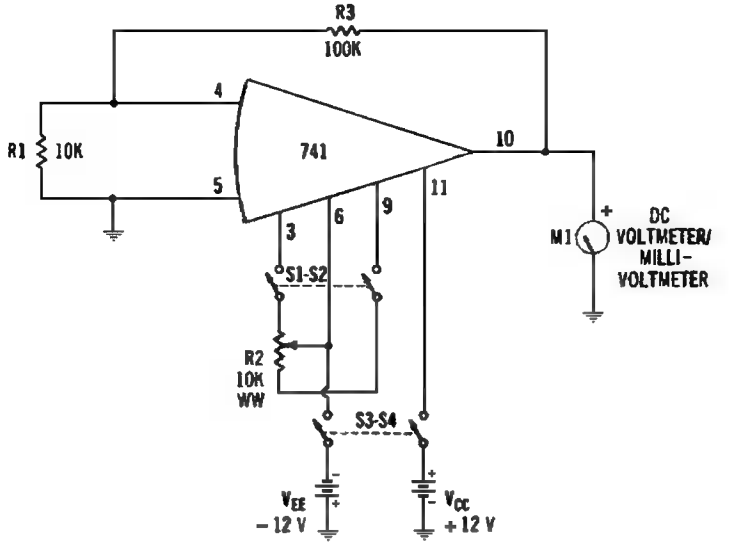


Fig. 2-6. Offset-null adjustment, internal.

1 dpst switch (S2-S3)
1 10K wirewound potentiometer (R1)
1 10-ohm resistor (R2)
1 10K resistor (R3)
1 100K resistor (R4)
1 +12 V dc supply (V_{CC})

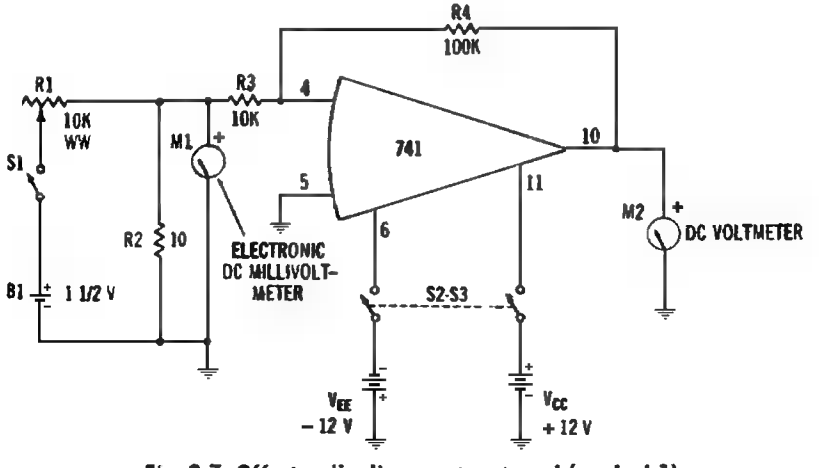


Fig. 2-7. Offset-null adjustment, external (method 1).

1 −12 V dc supply (V_{EE})
1 1½ V size-C cell (B1)

Step 3 (Fig. 2-8)

1 741 integrated circuit
1 electronic dc millivoltmeter (M1)
1 dc voltmeter (M2)
1 spst switch (S1)
1 dpst switch (S2-S3)
1 10K wirewound potentiometer (R1)
1 10-ohm resistor (R2)
1 100K resistor (R3)
1 +12 V dc supply (V_{CC})
1 −12 V dc supply (V_{EE})
1 1½ V size-C cell (B1)

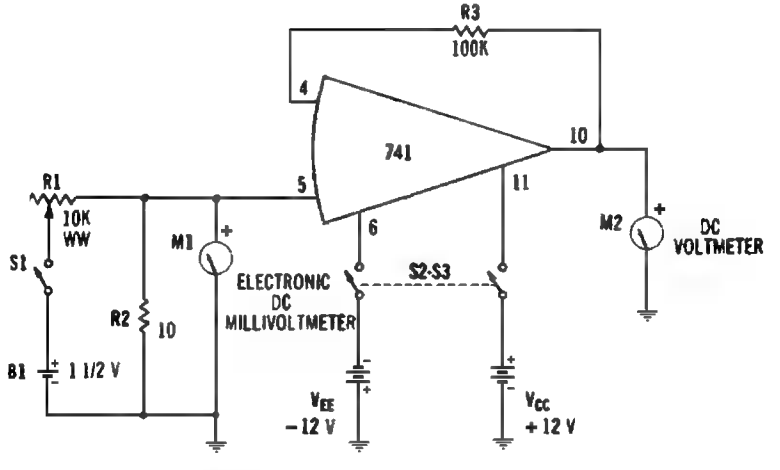


Fig. 2-8. Offset-null adjustment, external (method 2).

Test Procedure

This experiment actually involves three test procedures, Steps 1, 2, and 3 below.

Step 1. Internal

This method employs a zero-set potentiometer connected between the offset-null terminals of the IC.

1. With switches S1-S2 and S3-S4 open and with potentiometer R2 set to midrange, set up the test circuit as shown in Fig. 2-6.

2. Close switch S3-S4. Note that the meter is slightly deflected owing to offset (Experiment 3).
3. Close switch S1-S2, and adjust potentiometer R2 to set the deflection to zero.

Step 2. External (Method 1)

This method employs an external nulling voltage applied to the inverting input (terminal 4) of the IC.

1. With switches S1 and S2-S3 open and with potentiometer R1 set to maximum resistance, set up the test circuit as shown in Fig. 2-7.
2. Close switch S2-S3. Note that meter M2 deflects, indicating offset.
3. Close switch S1, and slowly adjust potentiometer R1 to apply a positive input-signal voltage (indicated by millivoltmeter M1). Note that this reduces the reading of voltmeter M2.
4. Continue adjustment of R1 until M2 reads zero. At this point, read from meter M1 the voltage required to null the offset through the inverting input of the IC.

Step 3. External (Method 2)

This method employs an external nulling voltage applied to the noninverting input (terminal 5) of the IC.

1. With switches S1 and S2-S3 open and potentiometer R1 set to maximum resistance, set up the test circuit as shown in Fig. 2-8.
2. Close switch S2-S3. Note that meter M2 deflects, indicating offset.
3. Close switch S1, and slowly adjust potentiometer R1 to apply a positive input-signal voltage (indicated by millivoltmeter M1) Note that this reduces the reading of voltmeter M2.
4. Continue adjustment of R1 until M2 reads zero. At this point, read from meter M1 the voltage required to null the offset through the noninverting input of the IC.

Sample Results

Step 2: Input null voltage = 1 mV
Step 3: Input null voltage = 10 mV

EXPERIMENT 6. INPUT OFFSET VOLTAGE

Required Equipment (Fig. 2-9)

1 741 integrated circuit
1 electronic dc millivoltmeter (M1)
1 dc voltmeter (M2)

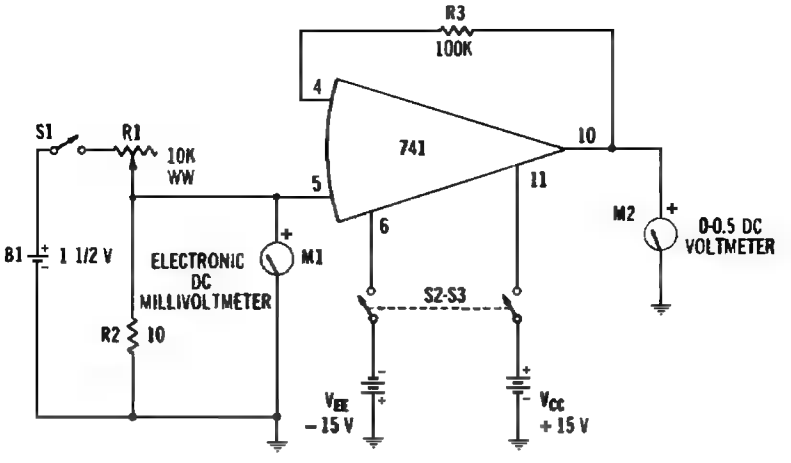


Fig. 2-9. Input offset voltage.

1 spst switch (S1)
1 dpst switch (S2-S3)
1 10K wirewound potentiometer (R1)
1 10-ohm resistor (R2)
1 100K resistor (R3)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})
1 1½ V size-C cell (B1)

Test Procedure

1. With switches S1 and S2-S3 open and with potentiometer R1 set to maximum resistance, set up the test circuit as shown in Fig. 2-9.
2. Close switch S2-S3, noting that meter M2 is deflected by offset.
3. Close switch S1, and slowly adjust potentiometer R1 to set meter M2 to zero. At this point, note the deflection of meter M1; this voltage is equal to the input offset voltage which it balances out.

Sample Result

$V_{IO} = 1$ mV

EXPERIMENT 7. INPUT OFFSET CURRENT

Required Equipment (Fig. 2-10)

1 741 integrated circuit
1 low-range dc microammeter (M1)

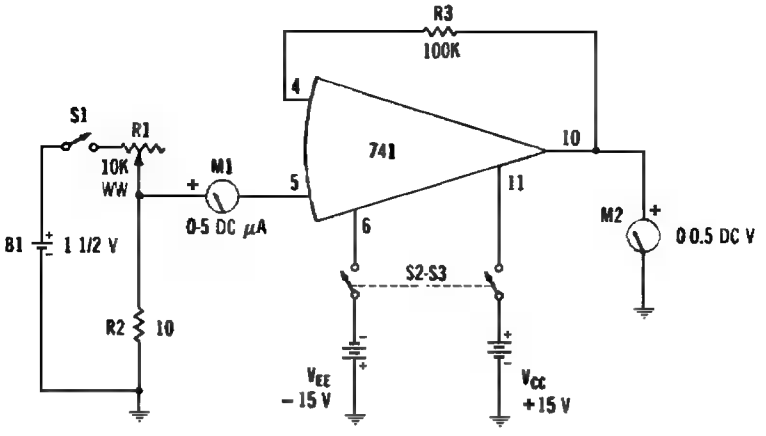


Fig. 2-10. Input offset current.

1 dc voltmeter (M2)
1 spst switch (S1)
1 dpst switch (S2-S3)
1 10K wirewound potentiometer (R1)
1 10-ohm resistor (R2)
1 100K resistor (R3)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})
1 1½ V size-C cell (B1)

Test Procedure

1. With switches S1 and S2-S3 open and with potentiometer R1 set to maximum resistance, set up the test circuit of Fig. 2-10.
2. Close switch S2-S3, noting that meter M2 is deflected by offset.
3. Close switch S1, and slowly adjust potentiometer R1 to set meter M2 to zero. At this point, note the deflection of meter M1; this reading is equal to the input offset current.

Sample Result

$I_{io} = 0.1\ \mu A = 100\ nA$

EXPERIMENT 8. CLOSED-LOOP DC VOLTAGE GAIN

Required Equipment (Figs. 2-11 and 2-12)

1 741 integrated circuit
2 dc voltmeters (M1, M2)

1 spst switch (S1)
1 dpst switch (S2-S3)
1 10K wirewound potentiometer (R1)
1 10K resistor (R2)
1 100K resistor (R3)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})
1 1½ V size-C cell (B1)

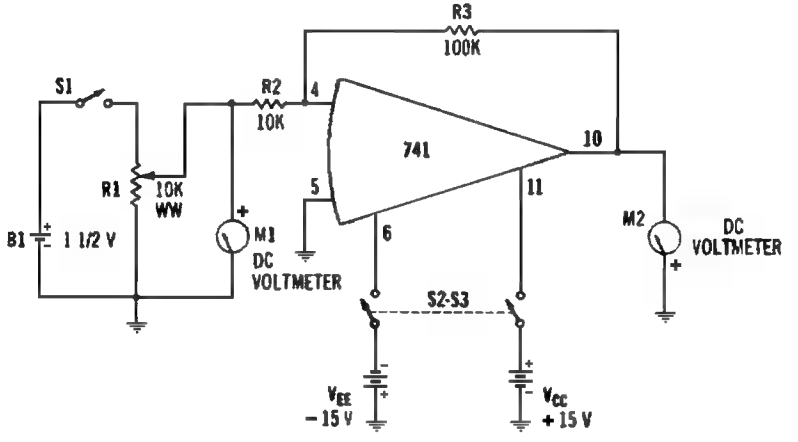


Fig. 2-11. Closed-loop dc voltage gain (inverting).

Test Procedure

This experiment actually involves two test procedures, Steps 1 and 2 below.

Step 1. Inverting

1. With switches S1 and S2-S3 open and with potentiometer R1 set to zero, set up the test circuit as shown in Fig. 2-11. Watch the meter polarity.
2. Close switch S2-S3. Observe that meter M2 is slightly deflected, owing to offset (Experiment 3).
3. Close switch S1, and adjust potentiometer R1 for a dc input signal (V_i) of 0.1 V indicated by meter M1.
4. Read the corresponding dc output-signal voltage (V_o) indicated by meter M2. Note that the output-signal polarity is negative, whereas the input-signal polarity is positive. This is the result of signal inversion in the IC.
5. Calculate the voltage gain: $A = V_o/V_i$.

6. Note that A also equals R3/R2, the ratio of feedback resistance to input resistance. Check the gain with various other values of resistance substituted for the original 100K.

Step 2. Noninverting

1. With switches S1 and S2-S3 open and with potentiometer R1 set to zero, set up the test circuit as shown in Fig. 2-12. Watch the meter polarity.
2. Close switch S2-S3. Observe that meter M2 is slightly deflected, owing to offset (Experiment 3).

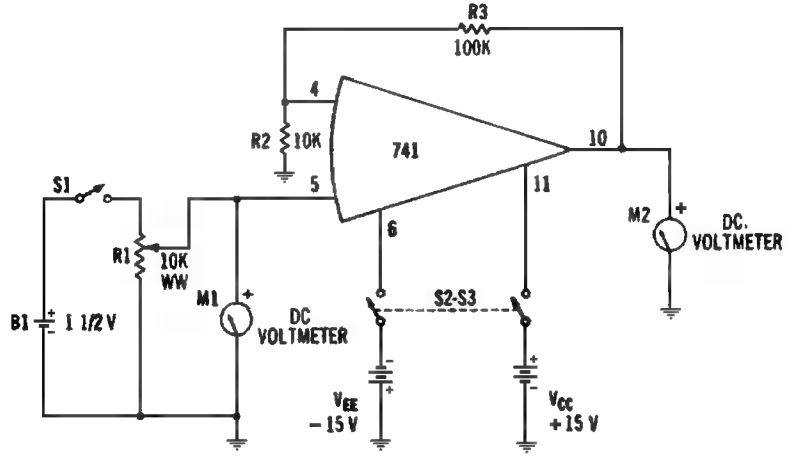


Fig. 2-12. Closed-loop dc voltage gain (noninverting).

3. Close switch S1, and adjust potentiometer R1 for a dc input signal (V_i) of 0.1 V indicated by meter M1.
4. Read the corresponding dc output signal (V_o) indicated by meter M2. Note that the output-signal polarity is positive, the same as the input signal (noninversion in the IC).
5. Calculate the voltage gain: $A = V_o/V_i$.
6. Note that A also equals R3/R2, the ratio of feedback resistance to input resistance. Check the gain with various other values of resistance substituted for the original 100K.

Sample Results

Step 1: $A = V_o/V_i = 1/0.1 = 10$, inverting
Step 2: $A = V_o/V_i = 1/0.1 = 10$, noninverting

EXPERIMENT 9. OPEN-LOOP AC VOLTAGE GAIN

Required Equipment (Fig. 2-13)

1 741 integrated circuit
1 electronic ac millivoltmeter (M1)
1 electronic ac voltmeter (M2)—*optional*
1 voltage-calibrated oscilloscope
1 sine-wave generator
2 0.1-μF capacitors (C1, C2)
1 dpst switch (S1-S2)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})

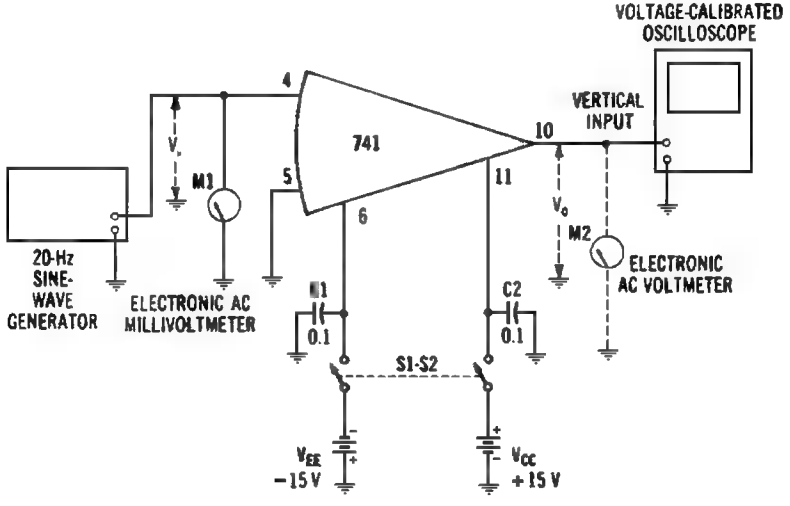


Fig. 2-13. Open-loop ac voltage gain.

Test Procedure

1. With switch S1-S2 open, the generator off and its output attenuator set to zero, and the oscilloscope off, set up the test circuit as shown in Fig. 2-13. (In this experiment, the IC runs "wide open" and is "touchy." Keep all leads short and direct.)
2. Close switch S1-S2, switch on the generator, and switch on the oscilloscope.
3. Set the generator to 20 Hz.
4. Set the generator output (input signal V_i) for maximum undistorted output (V_o) indicated by the oscilloscope. Read the corresponding input-signal voltage (V_i) from meter M1. (Alterna-

tively, output voltage V_o may be read with an electronic ac voltmeter, M2. However, the meter does not readily show the exact point at which distortion of V_o begins.)

5. Calculate the voltage gain: $A = V_o/V_i$. (Both V_o and V_i must be in the same kind of units; that is, both must be in volts rms, volts peak, etc.)

Sample Result

$V_i = 0.3$ mV
$V_o = 1$ V
$A = 3333$

This is not the maximum amplification obtainable with open-loop operation. Individual ICs and individual test setups can afford much higher values than the above sample. Note also that this is the low-frequency (20-Hz) gain, relatively close to dc; open-loop gain falls rapidly with frequency (see Experiment 11).

EXPERIMENT 10. CLOSED-LOOP AC VOLTAGE GAIN

Required Equipment (Fig. 2-14)

1 741 integrated circuit
1 electronic ac voltmeter/millivoltmeter (M1)
1 sine-wave generator

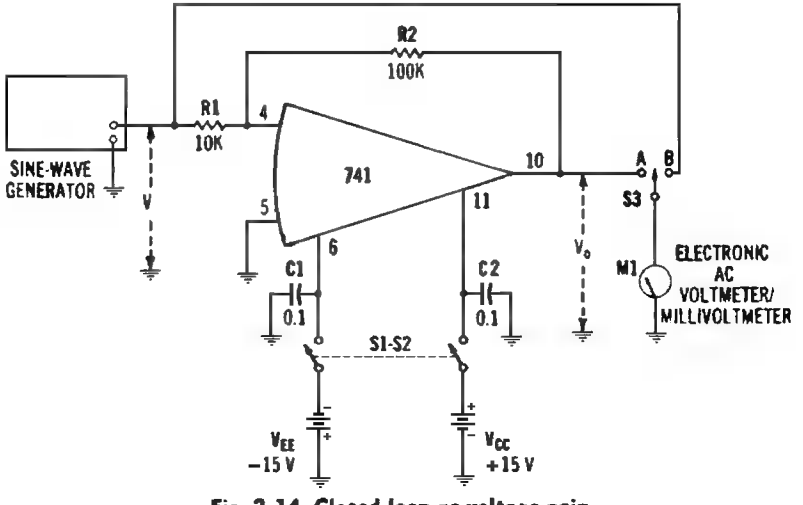


Fig. 2-14. Closed-loop ac voltage gain.

2 0.1-μF capacitors (C1, C2)
1 dpst switch (S1-S2)
1 spdt switch (S3)
1 10K resistor (R1)
1 100K resistor (R2)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})

Test Procedure

1. With switch S1-S2 open, switch S3 in position B, and the generator off and its attenuator set to zero, set up the test circuit as shown in Fig. 2-14.
2. Close switch S1-S2, and switch on the generator.
3. Set the generator to 1000 Hz.
4. Set the generator output (input signal V_i) to 0.1 V indicated by meter M1. Record V_i.
5. Throw switch S3 to position A, and read the corresponding output signal (V_o) indicated by meter M1. Record V_o.
6. Calculate the voltage gain: $A = V_o/V_i$.
7. Note that A also equals R2/R1, the ratio of feedback resistance to input resistance. Check the gain with various other values of resistance substituted for the original 100K.

Sample Result

$V_i = 0.1$ V
$V_o = 1$ V
$A = 10$

EXPERIMENT 11. OPEN-LOOP FREQUENCY RESPONSE

Required Equipment (Fig. 2-15)

1 741 integrated circuit
1 electronic ac millivoltmeter (M1)
1 electronic ac voltmeter (M2)—*optional*
1 voltage-calibrated oscilloscope
1 sine-wave generator
2 0.1-μF capacitors (C1, C2)
1 dpst switch (S1-S2)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})

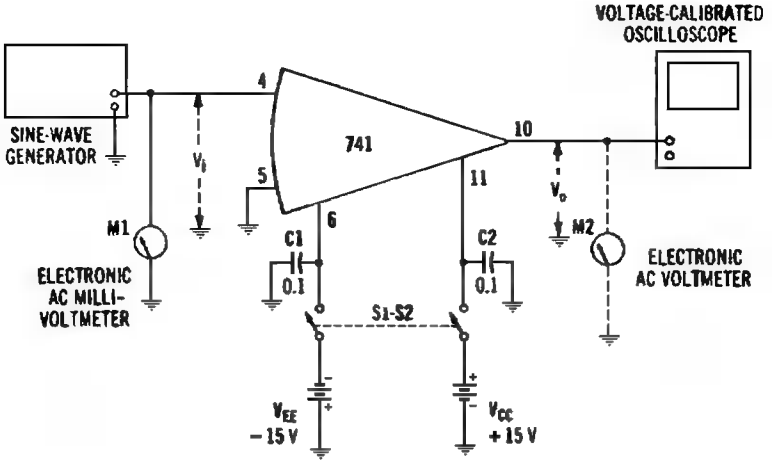


Fig. 2-15. Open-loop frequency response.

Test Procedure

1. With switch S1-S2 open, the generator off and its output attenuator set to zero, and the oscilloscope off, set up the test circuit as shown in Fig. 2-15. (In this experiment, the IC runs "wide open" and is "touchy." Keep all leads short and direct.)
2. Close switch S1-S2, and switch on the generator and oscilloscope
3. Set the generator to 20 Hz.
4. Set the generator output (input signal V_i) for maximum undistorted output signal (V_o) indicated by the oscilloscope. Read V_o from the calibrated vertical axis of the oscilloscope, and read the corresponding input signal (V_i) from meter M1. (Alternatively, V_o may be read with an electronic voltmeter M2. However, this meter will not readily show the exact point at which V_o becomes distorted.)

Table 2-2. Sample Results, Open-Loop Frequency Response

f	V_i	V_o	A_v
20 Hz	0.3 mV	1 V	3333
200 Hz	1 mV	1 V	1000
2 kHz	7 mV	1 V	142
20 kHz	20 mV	1 V	50
200 kHz	0.1 V	1 V	10

5. Calculate voltage gain: $A = V_o/V_i$. (Both V_o and V_i must be in the same kind of units; that is, both must be in volts rms, volts peak, etc.)
6. Repeat Steps 4 and 5 at frequencies of 200 Hz, 2 kHz, 20 kHz, and 200 kHz.

Sample Results

See Table 2-2.

EXPERIMENT 12. CLOSED-LOOP FREQUENCY RESPONSE

Required Equipment (Fig. 2-16)

1 741 integrated circuit
1 electronic ac voltmeter/millivoltmeter (M1)
1 sine-wave generator
2 0.1-μF capacitors (C1, C2)
1 10K resistor (R1)
1 100K resistor (R2)
1 dpst switch (S1-S2)
1 spdt switch (S3)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})

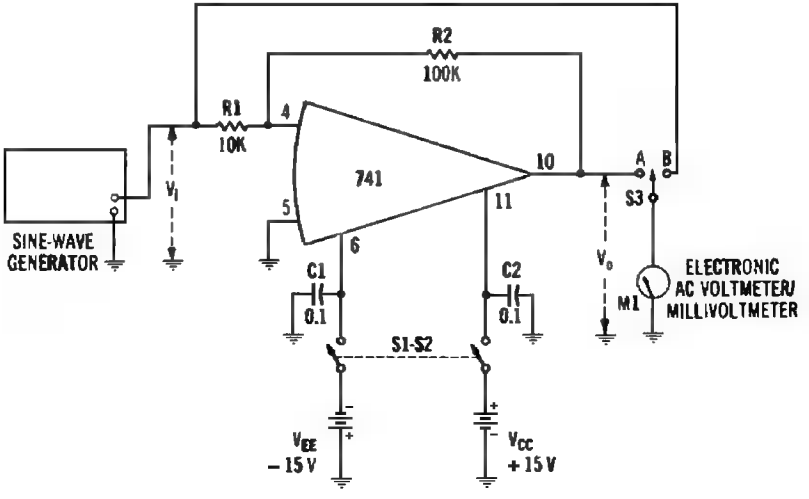


Fig. 2-16. Closed-loop frequency response.

Test Procedure

1. With switch S1-S2 open, switch S3 set to position B, and the generator off and its output attenuator set to zero, set up the test circuit as shown in Fig. 2-16.
2. Close switch S1-S2, and switch on the generator.
3. Set the generator to 20 Hz.
4. Set the generator output (input signal V_i) to 0.1 V as indicated by meter M1. Record V_i.
5. Throw switch S3 to position A and read the corresponding output signal (V_o) indicated by meter M1. Record V_o.
6. Calculate the voltage gain: $A = V_o/V_i$.
7. Repeat Steps 4, 5, and 6 at 200 Hz, 2 kHz, 20 kHz, and 200 kHz.

Sample Results

See Table 2-3.

Table 2-3. Sample Results, Closed-Loop Frequency Response

f	V_i	V_o	A
20 Hz	0.1 V	1 V	10
200 Hz	0.1 V	1 V	10
2 kHz	0.1 V	1 V	10
20 kHz	0.1 V	1.2 V	12
200 kHz	0.1 V	0.2 V	2

EXPERIMENT 13. UNITY-GAIN FREQUENCY

Required Equipment (Fig. 2-17)

1 741 integrated circuit
2 electronic ac voltmeter/millivoltmeters (M1, M2)
1 sine-wave generator (This instrument must furnish signals from 20 Hz to beyond 1 MHz; otherwise, two separate generators—one af, one rf—will be needed.)
2 0.1-μF capacitors (C1, C2)
1 dpst switch (S1-S2)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})

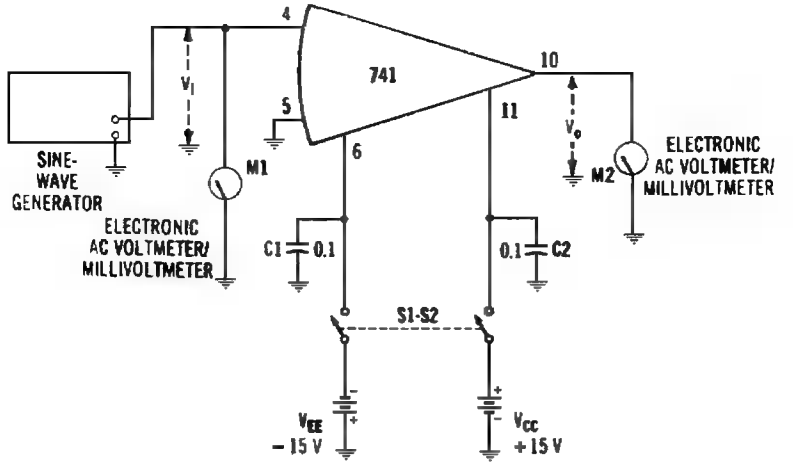


Fig. 2-17. Unity-gain frequency.

Test Procedure

1. With switch S1-S2 open and the generator off and its attenuator set to zero, set up the test circuit as shown in Fig. 2-17. (In this circuit, the IC runs "wide open" and is "touchy." Keep all leads short and direct.)
2. Close switch S1-S2, and switch on the generator.
3. Set the generator to 20 Hz.
4. Set the generator output (V_i) to 10 mV as indicated by M1.
5. Note the corresponding output voltage (V_o) indicated by meter M2. Calculate the 20-Hz voltage gain: $A = V_o/V_i$.
6. While holding input signal V_i to 10 mV, tune the generator through its range. Note the frequency at which voltage gain $A = 1$ ($V_o = 10$ mV). This is the unity-gain frequency of the IC.

Sample Result

f = 1 MHz

EXPERIMENT 14. MAXIMUM DC OUTPUT-VOLTAGE SWING

Required Equipment (Fig. 2-18)

1 741 integrated circuit
2 dc voltmeters (M1, M2)

1 10K wirewound potentiometer (R1)
1 10K resistor (R2)
1 100K resistor (R3)
1 spst switch (S1)
1 dpst switch (S2-S3)
1 +12 V dc supply (V_{CC})
1 −12 V dc supply (V_{EE})
1 1½ V size-C cell (B1)

Test Procedure

1. With switches S1 and S2-S3 open and with potentiometer R1 set to zero, set up the test circuit as shown in Fig. 2-18.
2. Close switch S2-S3.
3. Close switch S1, and adjust potentiometer R1 for an input signal (V_i) of 0.1 V as indicated by meter M1. Record V_i
4. Read the corresponding output-signal voltage (V_o) indicated by meter M2. Record V_o.
5. Repeat Steps 3 and 4 in 0.1-volt steps of input voltage until further increase of V_i causes no change in V_o (see last four entries in Table 2-4). The lowest point at which this V_o saturation occurs is the maximum dc output-voltage swing.

Sample Results

$V_{o\ max}$ = 10 V dc (See Table 2-4.)

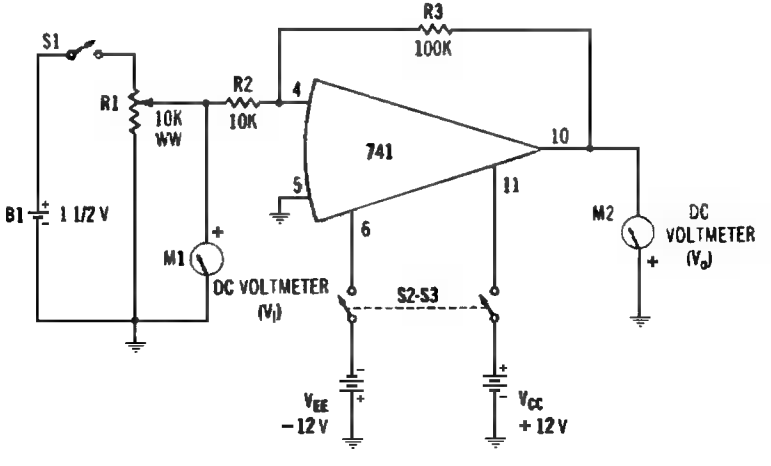


Fig. 2-18. Maximum dc output-voltage swing.

Table 2-4. Sample Results, Maximum DC Output-Voltage Swing

V_i	V_o	
0.1 V	1.0 V	
0.2 V	2.0 V	
0.3 V	3.0 V	
0.4 V	4.0 V	
0.5 V	5.0 V	
0.6 V	6.0 V	
0.7 V	7.0 V	
0.8 V	8.0 V	
0.9 V	9.0 V	
1.0 V	9.8 V	
1.1 V	10.0 V	Saturation
1.2 V	10.0 V	
1.3 V	10.0 V	
1.4 V	10.0 V	

This is the condition for dc = ±12 V, and R3/R2 = 10.

EXPERIMENT 15. MAXIMUM AC OUTPUT-VOLTAGE SWING

Required Equipment (Fig. 2-19)

1 741 integrated circuit
1 sine-wave generator
1 voltage-calibrated oscilloscope
1 electronic ac voltmeter (M1)—*optional*
2 0.1-μF capacitors (C1, C2)
1 10K resistor (R1)
1 100K resistor (R2)
1 dpst switch (S1-S2)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})

Test Procedure

1. With switch S1-S2 open, the oscilloscope off, and the generator off and its output attenuator set to zero, set up the test circuit as shown in Fig. 2-19.
2. Close switch S1-S2, and switch on the generator and oscilloscope.
3. Set the generator to 1000 Hz.

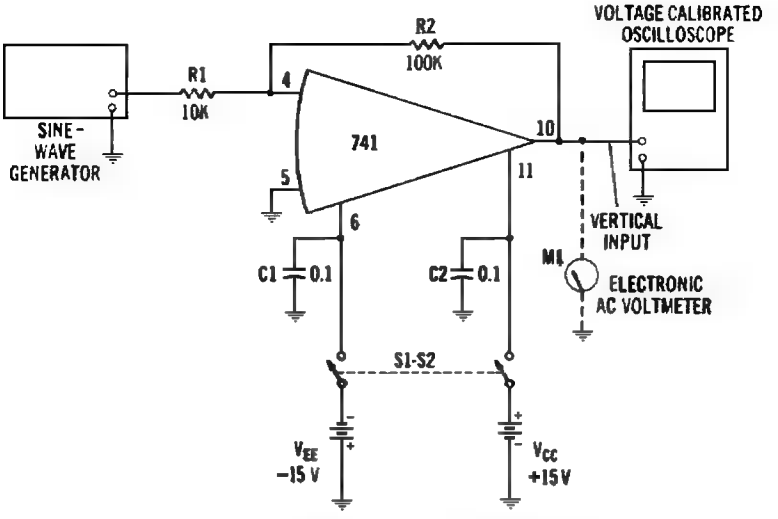


Fig. 2-19. Maximum ac output-voltage swing.

4. Adjust the generator output for maximum undistorted IC output signal, as indicated by the oscilloscope.
5. Read the output voltage (V_o) from the oscilloscope. This value is the maximum output-voltage swing with the IC operating from 15-volt dc supplies and with R2/R1 = 10. (Alternatively, an electronic ac voltmeter, M1, might be used to read the output voltage; however, this meter will not readily show the exact point at which the output voltage becomes distorted.)

Sample Result

V_o = 5.2 V rms = 7.35 V peak = 14.7 V peak-to-peak

EXPERIMENT 16. DC INPUT-VOLTAGE RANGE

Required Equipment (Fig. 2-20)

1 741 integrated circuit
2 dc voltmeters (M1, M2)
1 10K wirewound potentiometer (R1)
1 10K resistor (R2)
1 100K resistor (R3)
1 spst switch (S1)
1 dpst switch (S2-S3)
1 +12 V dc supply (V_{cc})

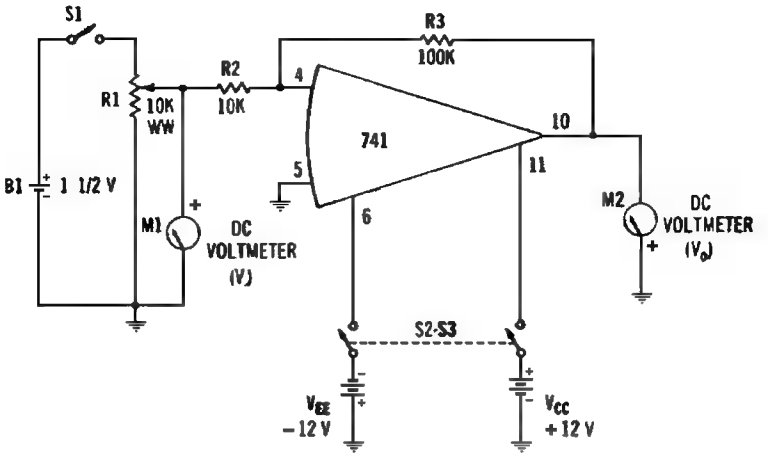


Fig. 2-20. Dc input-voltage range.

1 −12 V dc supply (V_{EE})
1 1½ V size-C cell (B1)

Test Procedure

1. With switches S1 and S2-S3 open and with potentiometer R1 set to zero, set up the test circuit as shown in Fig. 2-20.
2. Close switch S2-S3.
3. Close switch S1, and adjust potentiometer R1 to increase slowly input signal V_i (as indicated by meter M1).
4. Continue to increase V_i while observing the deflection of meter M2 (output-signal voltage V_o).
5. Increase V_i to the point at which output voltage V_o shows no further increase, but levels off. The value of V_i at this point is the maximum input-signal voltage for the conditions dc supply = ±12 V and R3/R2 = 10.

Sample Result

V_i = 1.1 V for V_o = 10 V (saturated)
Dc input voltage range = 0–1.1 V

EXPERIMENT 17. AC INPUT-VOLTAGE RANGE

Required Equipment (Fig. 2-21)

1 741 integrated circuit
1 sine-wave generator

1 electronic ac voltmeter/millivoltmeter (M1)
1 oscilloscope
2 0.1-μF capacitors (C1, C2)
1 10K resistor (R1)
1 100K resistor (R2)
1 dpst switch (S1-S2)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})

Test Procedure

1. With switch S1-S2 open, the oscilloscope off, and the generator off (with its output attenuator set to zero), set up the test circuit as shown in Fig. 2-21.
2. Close switch S1-S2, and switch on the generator and oscilloscope.
3. Set the generator to 1000 Hz.
4. Adjusting the attenuator, slowly increase the output of the generator to the point at which peak clipping just begins in the IC output signal, as shown by the oscilloscope.
5. At this point, read the corresponding input signal (V_i) from meter M1. This value of V_i is the upper limit of the input-voltage range for the conditions dc supply = ±15 V and R2/R1 = 10.

Sample Results

V_i = 0.5 V rms = 0.71 V peak = 1.41 V peak-to-peak

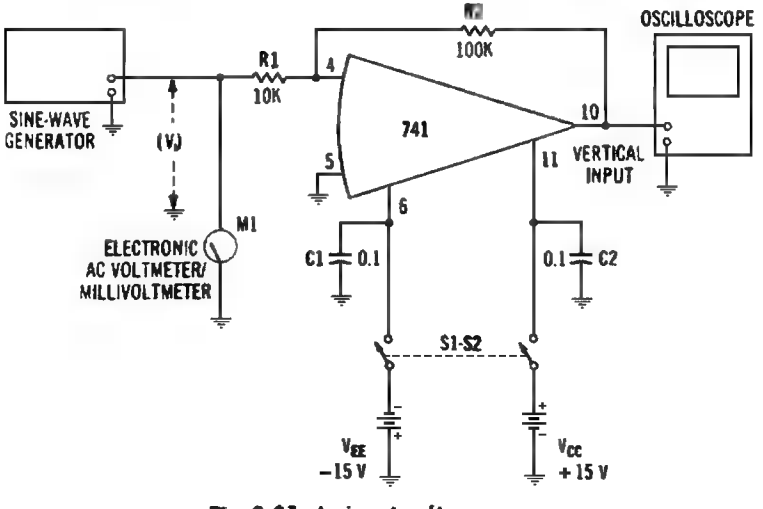


Fig. 2-21. Ac input-voltage range.

EXPERIMENT 18. COMMON-MODE REJECTION

Required Equipment (Fig. 2-22)

1 741 integrated circuit
1 sine-wave generator
2 electronic ac voltmeter/millivoltmeters (M1, M2)
1 1-μF capacitor (C1)
2 0.1-μF capacitors (C2, C3)
1 500-ohm resistor (R1)
1 dpst switch (S1-S2)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})

Test Procedure

1. With switch S1-S2 open and the generator off (with its output attenuator set to zero), set up the test circuit as shown in Fig. 2-22.
2. Close switch S1-S2, and turn on the generator.
3. Set the generator to 20 Hz.
4. Adjust the generator attenuator for two selected successive values of input-signal voltage V_i, as indicated by meter M1. Record these as V_{i1} and V_{i2}.
5. Read the corresponding output-signal voltages from meter M2. (This output represents the signal transmitted by the IC as a result of offset.) Record these as V_{o1} and V_{o2}.

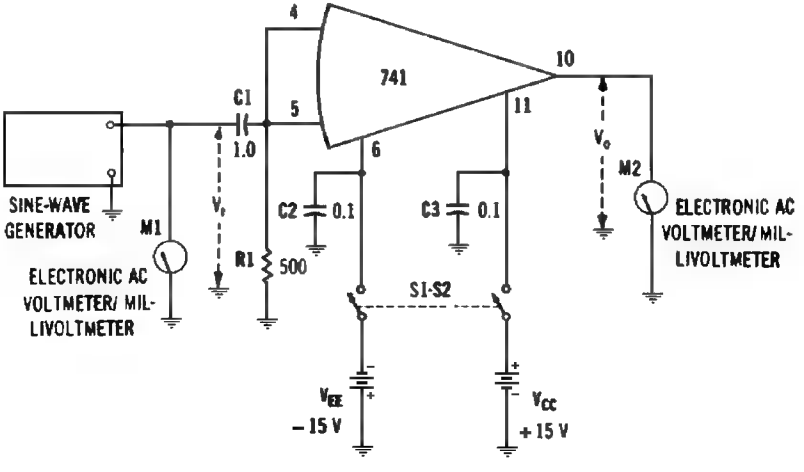


Fig. 2-22 Common-mode rejection.

6. Calculate the input-signal increment: $\Delta V_i = V_{i2} - V_{i1}$.
7. Calculate the output-signal increment: $\Delta V_o = V_{o2} - V_{o1}$.
8. Calculate the ratio $\Delta V_i / \Delta V_o$. Convert the resulting value to minus decibels.
9. Set the generator to 10 kHz, and repeat Steps 4 through 8.
10. Set the generator to 100 kHz, and repeat Steps 4 through 8.
11. Note that V_o increases with frequency, showing that common-mode rejection decreases as the frequency increases.

Sample Results

Common-Mode Rejection = −82.5 dB at 20 Hz
−78.4 dB at 10 kHz
−49.7 dB at 100 kHz

EXPERIMENT 19. DC FOLLOWER OPERATION

Required Equipment (Fig. 2-23)

1 741 integrated circuit
1 dc microammeter (M1)
1 dc voltmeter (M2)
1 10K wirewound potentiometer (R1)
1 200-ohm wirewound potentiometer (R2)
1 spst switch (S1)
1 dpst switch (S2-S3)
1 spdt switch (S4)
1 +15 V dc supply (V_{CC})

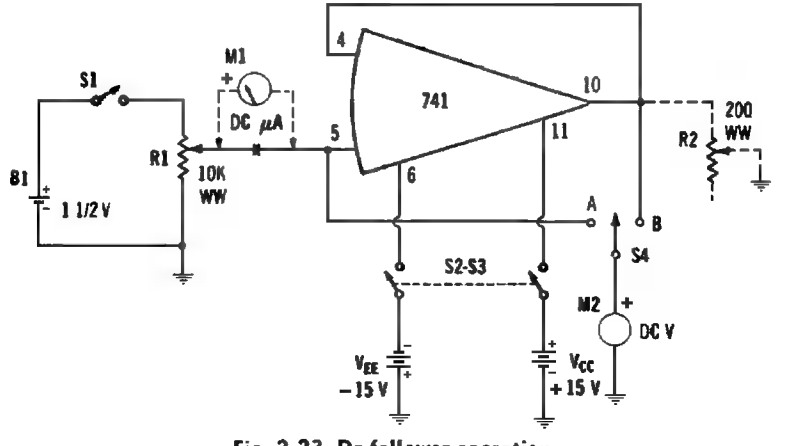


Fig. 2-23. Dc follower operation.

1 −15 V dc supply (V_{EE})
1 1½ V size-C cell (B1)

Test Procedure

Note that 100% feedback is provided by the connection between output terminal 10 and inverting input terminal 4.

1. With switches S1 and S2-S3 open, switch S4 set to position A, and potentiometer R1 set to zero, set up the test circuit as shown in Fig. 2-23.
2. Close switch S2-S3.
3. Close switch S1, and set potentiometer R1 for a convenient value of input-signal voltage V_i, as indicated by voltmeter M2.
4. Throw switch S4 to position B, and read corresponding output voltage V_o from voltmeter M2. Note that V_o has the same value as V_i and the same polarity.
5. Calculate the voltage gain: $A = V_o/V_i = 1$.
6. Repeat Steps 3 through 5 at a number of selected values of input voltage V_i.
7. Temporarily insert the dc microammeter as shown by dash lines. Note that the input-signal current is scarcely discernible at any of the V_i values.
8. Temporarily connect 200-ohm potentiometer R2 from output terminal 10 to ground, as shown by dash lines. At any one of the output voltages (Step 4, above), adjust R2 to the point at which V_o falls to one-half its value. At this point, the IC-follower output resistance equals the R2 setting.

Sample Results

$A = 1.0$
$R_o = 30$ ohms

EXPERIMENT 20. AC FOLLOWER OPERATION

Noninverting Type

Required Equipment (Fig. 2-24)

1 741 integrated circuit
1 sine-wave generator
1 voltage-calibrated oscilloscope
1 electronic ac voltmeter (M1)—*optional*
2 0.1-μF capacitors (C1, C2)
1 dpst switch (S1-S2)

1 spdt switch (S3)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})

Test Procedure

1. With switch S1-S2 open, switch S3 set to position B, the oscilloscope and generator off, and the generator output attenuator set to zero, set up the test circuit as shown in Fig. 2-24.
2. Set the generator to 1000 Hz.
3. Close switch S1-S2, switch on the generator, and switch on the oscilloscope.

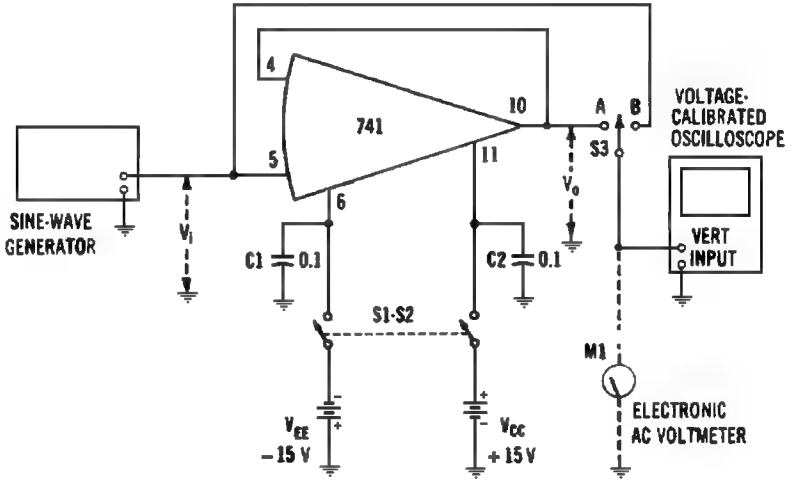


Fig. 2-24. Ac follower operation (noninverting).

4. Adjust the generator output attenuator for a convenient input-signal voltage, V_i, as indicated by the oscilloscope or meter M1.
5. Throw switch S3 to position A, and read the corresponding output voltage, V_o, as indicated by the oscilloscope or meter M1.
6. Note that $V_o = V_i$, and that voltage amplification $A = V_o/V_i = 1$. Note also that output signal V_o is in phase with input voltage V_i.
7. Repeat Steps 4 through 6 at other frequencies.

Sample Results

$V_o = V_i = 3$ V rms
$A = V_o/V_i = 1.0$

Inverting Type

Since the output-signal polarity here is the opposite of the input-signal polarity, this circuit (Fig. 2-25) might not be regarded as a follower at all, but simply as an inverting amplifier with unity gain.

Required Equipment (Fig. 2-25)

1 741 integrated circuit
1 sine-wave generator
1 voltage-calibrated oscilloscope
1 electronic ac voltmeter (M1)—*optional*
2 0.1-μF capacitors (C1, C2)
2 10K resistors (R1, R2)
1 dpst switch (S1-S2)
1 spdt switch (S3)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})

Test Procedure

1. With switch S1-S2 open, switch S3 set to position B, the oscilloscope and generator off, and the generator output attenuator set to zero, set up the test circuit as shown in Fig. 2-25.
2. Set the generator to 1000 Hz.
3. Close switch S1-S2, and switch on the generator and oscilloscope.
4. Adjust the generator output attenuator for a convenient input-signal voltage, V_i, as indicated by the oscilloscope or meter M1.
5. Throw switch S3 to position A, and read the corresponding output-signal voltage, V_o, as indicated by the oscilloscope or meter M1.
6. Note that $V_o = V_i$, and that voltage amplification $A = V_o/V_i = 1$. Note also that V_o is 180° out of phase with V_i.
7. Repeat Steps 4 through 6 at other frequencies.

Sample Results

$V_o = V_i = 2.1$ V rms
$A = V_o/V_i = 1.0$

EXPERIMENT 21. INPUT IMPEDANCE

Required Equipment (Fig. 2-26)

1 741 integrated circuit
1 sine-wave generator

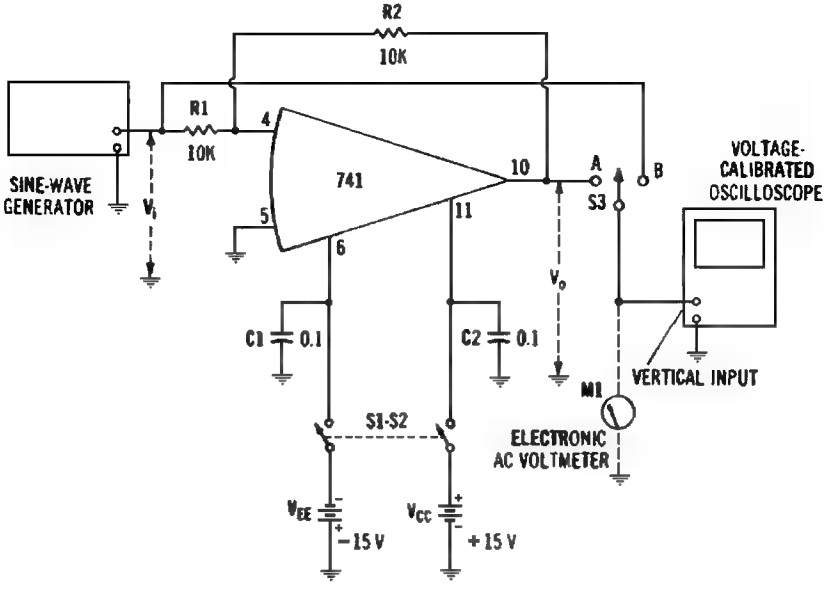


Fig. 2-25. Ac follower operation (inverting).

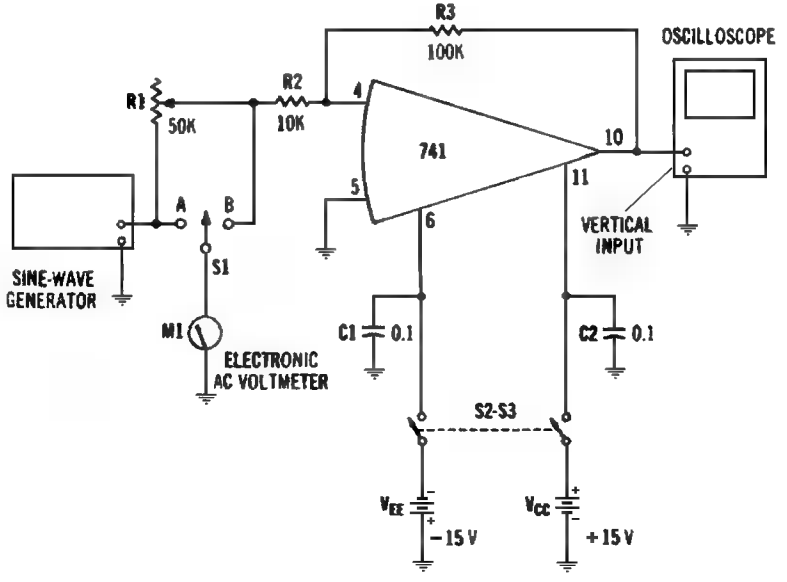


Fig. 2-26. Input impedance.

1 voltage-calibrated oscilloscope
1 electronic ac voltmeter (M1)
2 0.1-μF capacitors (C1, C2)
1 50K potentiometer (R1)
1 10K resistor (R2)
1 100K resistor (R3)
1 spdt switch (S1)
1 dpst switch (S2-S3)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})

Test Procedure

1. With switch S1 set to position A, switch S2-S3 open, potentiometer R1 set to zero, the oscilloscope and generator off, and the generator output attenuator set to zero, set up the test circuit as shown in Fig. 2-26.
2. Set the generator to 1000 Hz.
3. Close switch S2-S3, switch on the generator, and switch on the oscilloscope.
4. Adjust the generator output attenuator for maximum undistorted output signal, as indicated by the oscilloscope. Note the reading (V_1) of meter M1.
5. Without disturbing the setting of the attenuator, throw switch S1 to position B. This changes the deflection of meter M1, but only slightly.
6. Increase the resistance setting of potentiometer R1 to reduce V_1 to one-half the original value obtained in Step 4.
7. At this point, the input impedance (Z_i) of the IC is equal to the resistance setting of potentiometer R1.
8. Repeat Steps 4 through 7 at other frequencies.

Sample Results

$V_1 = 0.3$ V rms
$Z_i = 5000$ ohms

EXPERIMENT 22. OUTPUT IMPEDANCE

Required Equipment (Fig. 2-27)

1 741 integrated circuit
1 sine-wave generator
1 voltage-calibrated oscilloscope

5. Close switch S3. Note that this disturbs the deflection of meter M1 or the height of the pattern on the oscilloscope screen.
6. Adjust potentiometer R3 to restore output voltage V_o to its original value obtained in Step 4.
7. At this point, output impedance Z_o is equal to the resistance setting of potentiometer R3.
8. Repeat Steps 4 through 7 at other frequencies.

Sample Results

$V_o = 3$ V rms
$Z_o = 250$ ohms

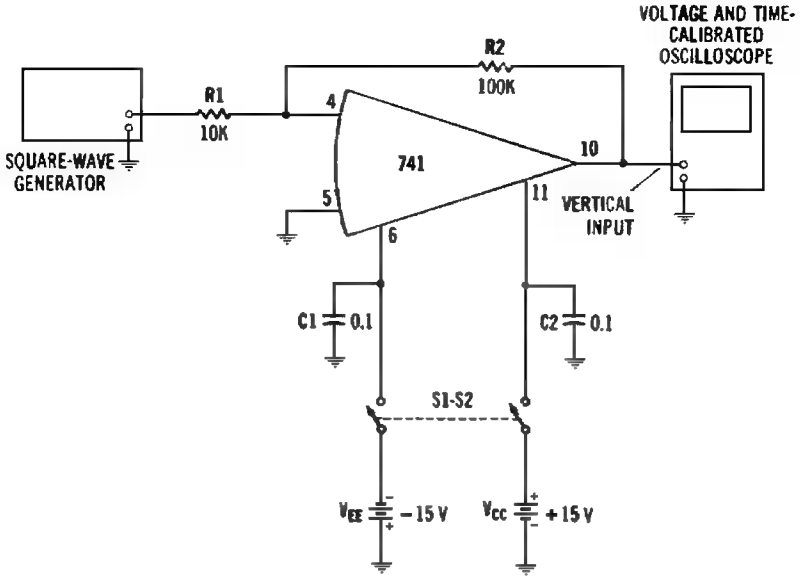
EXPERIMENT 23. SLEW RATE

Required Equipment (Fig. 2-28A)

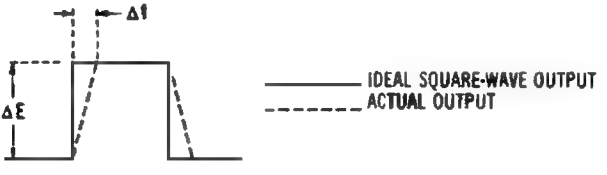
1 741 integrated circuit
1 square-wave generator
1 voltage- and time-calibrated oscilloscope
2 0.1-μF capacitors (C1, C2)
1 10K resistor (R1)
1 100K resistor (R2)
1 dpst switch (S1-S2)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})

Test Procedure

1. With switch S1-S2 open, the oscilloscope and generator off, and the generator output attenuator set to zero, set up the test circuit as shown in Fig. 2-28A.
2. Set the generator to 20 Hz.
3. Close switch S1-S2, and switch on the generator and oscilloscope.
4. Increase the setting of the generator attenuator, and adjust the oscilloscope controls for a single square wave on the screen.
5. Continue to increase the output of the generator until the square wave distorts, as shown by the dash lines in Fig. 2-28B.
6. As shown in Fig. 2-28B, from the calibrated screen of the oscilloscope read IC output voltage ΔE in volts and rise time Δt in microseconds.
7. Calculate the slew rate: $SR = \Delta E/\Delta t$ volts per microsecond. Correct, if desired, by allowing for the inherent rise times of the generator and oscilloscope.



(A) Test setup.



(B) Response.

Fig 2-28. Slew rate.

Sample Result

SR = 0.5 V/μs

EXPERIMENT 24. CURRENT GAIN

Required Equipment (Fig. 2-29)

1 741 integrated circuit
1 dc microammeter (M1)
1 dc milliammeter (M2)
1 5-megohm potentiometer (R1)
1 100K resistor (R2)
1 spst switch (S1)

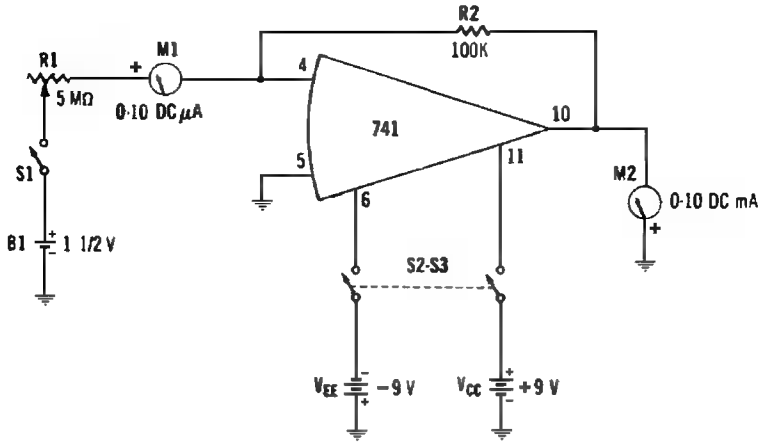


Fig. 2-29. Current gain.

1 dpst switch (S2-S3)
1 +9 V dc supply (V_{CC})
1 −9 V dc supply (V_{EE})
1 1½ V size-C cell (B1)

Test Procedure

1. With switches S1 and S2-S3 open and with potentiometer R1 set to maximum, set up the test circuit as shown in Fig. 2-29.
2. Close switch S2-S3.
3. Close switch S1.
4. Slowly decrease the resistance setting of potentiometer R1, noting that both meters begin to read.
5. Adjust potentiometer R1 for 1 μA of input current (I_i).
6. Note the corresponding output current (I_o) indicated by meter M2.
7. Calculate the current gain: $A_i = I_o/I_i$.

Typical Results

$I_i = 1\ \mu A$, $I_o = 4$ mA $= 4000\ \mu A$; $A_i = 4000/1 = 4000$

EXPERIMENT 25. POWER-SUPPLY REJECTION RATIO

Required Equipment (Fig. 2-30)

1 741 integrated circuit
1 electronic dc millivoltmeter (M1)

1 dc voltmeter (M2)
1 10K wirewound potentiometer (R1)
1 10-ohm resistor (R2)
1 100K resistor (R3)
1 spst switch (S1)
1 dpst switch (S2-S3)
1 0 to +15 V dc supply (V_{CC})
1 0 to −15 V dc supply (V_{EE})
1 1½ V size-C cell (B1)

Test Procedure

1. With switches S1 and S2-S3 open and with potentiometer R1 set to maximum resistance, set up the test circuit as shown in Fig. 2-30.
2. Set dc supplies V_{CC} and V_{EE} each to 15 V.
3. Close switch S2-S3, noting that output meter M2 deflects a small amount because of offset in the IC.
4. Close switch S1, and adjust potentiometer R1 to reduce the IC output (meter M2 deflection) to zero. At this point, record the deflection of meter M1 as V_{I1}.
5. Without disturbing the setting of potentiometer R1, reduce both V_{CC} and V_{EE} to 10 V.
6. If Step 5 causes meter M2 again to read, adjust potentiometer R1 to re-null M2. Record the corresponding reading of meter M1 as V_{I2}.

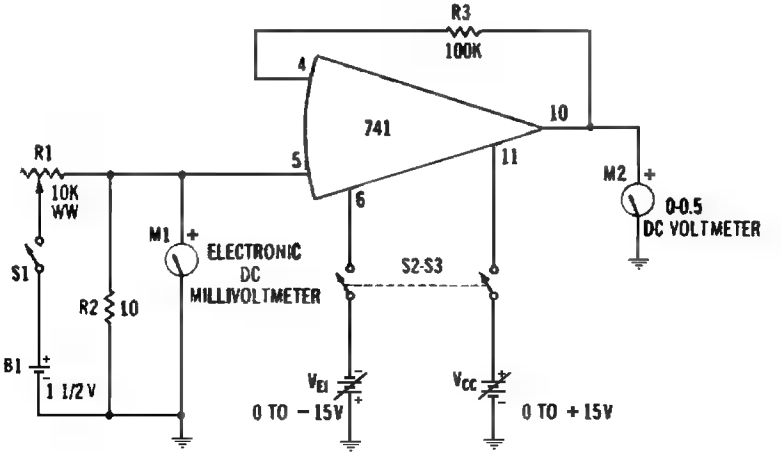


Fig. 2-30. Power-supply rejection ratio.

7. Calculate $\Delta V_i = V_{i2} - V_{i1}$. Record the result in microvolts.
8. Calculate the power-supply rejection ratio: $PSRR = \Delta V_i / \Delta V_s$, where ΔV_s = change in supply voltage (in this case, $15 - 10 = 5$ V).
9. Repeat Steps 2 through 8, first holding V_{CC} constant and changing V_{EE}, then by holding V_{EE} constant and changing V_{CC}. Note which of these supply-voltage changes affects the IC most.

Sample Results

$V_{i1} = 1$ mV
$V_{i2} = 1.25$ mV
$\Delta V_i = 0.25$ mV $= 250$ μV
$\Delta V_s = 15 - 10 = 5$ V
PSRR $= 250/5 = 50$ μV per volt

PART 3

Simple Applications

This part offers 41 simple, one-IC circuits which will allow the reader to see how the integrated circuit operates in some familiar applications. These circuits, which extend some of the experiments of Part 2, may be set up reasonably easily and, in addition to yielding performance data, may be retained for permanent use. No special assembly method is necessary. The reader is free to use permanent wiring, a plug-in breadboard, a clip-lead setup, or any other method, so long as the wiring is stationary and short. Some sensitive circuits, especially Fig. 3-4, require the shortest practicable input leads. The pointers given at the beginning of Part 2 apply as well here.

The dc drain of these circuits is very low, and the dc supplies may be either batteries or *low-ripple* ac-operated units. Dual power supplies are required in all circuits except Figs. 3-7 and 3-12, which operate with a single supply.

For testing circuit performance, use the same instruments and equipment employed in the experiments in Part 2.

Except where shown otherwise in the schematics or text.

1. All resistances are in ohms.
2. All fixed resistors are ¼-watt composition, 5% tolerance.
3. All potentiometers are composition, except where labeled *ww* (wirewound).
4. All capacitances are in microfarads (μF).
5. All capacitors are low-voltage nonelectrolytic.
6. Capacitors in frequency-determining networks—as in Figs. 3-10.

3-13, 3-14, 3-15, 3-16, and 3-17—are high-Q, close-tolerance mica or ceramic, except where a desired low-frequency operation requires high capacitances that are out of the mica range.

3.1 VOLTAGE-FOLLOWER AMPLIFIER

Fig. 3-1 shows the circuit of an ac voltage follower. This setup is equivalent to the vacuum-tube cathode follower, bipolar-transistor emitter follower, and FET source follower. Unlike the latter circuits, however, the IC follower gives a gain of exactly 1. Followers are very handy for transformerless up/down impedance transformation

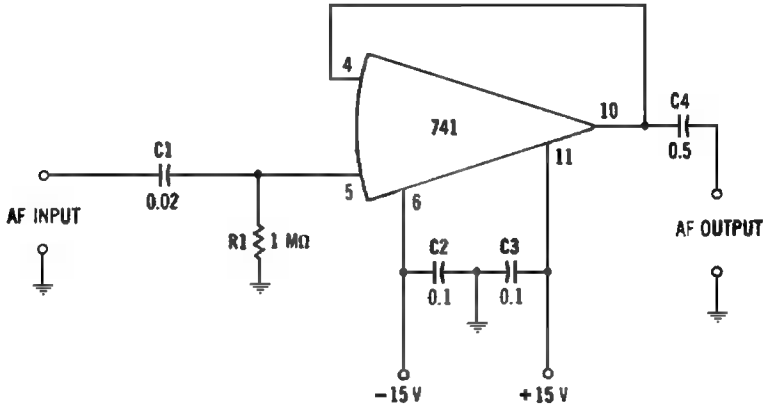


Fig. 3-1. Voltage-follower amplifier.

throughout electronics. In Fig. 3-1, 100% inverse feedback is provided by the direct connection between output terminal 10 and inverting-input terminal 4.

Check the circuit for (1) dc drain, (2) maximum input-signal amplitude, (3) maximum output-voltage swing, (4) input impedance, (5) output impedance, (6) voltage gain, (7) frequency response, (8) output/input phase, and (9) total harmonic distortion.

3.2 GAIN-OF-10 AUDIO AMPLIFIER

Fig. 3-2 shows the circuit of an audio amplifier having a voltage gain of 10. Here, the gain is set by negative feedback and is determined by the ratio of the 100K feedback resistance to the 10K input resistance ($A_v = R2/R1$). This unit is usable either as a main ampli-

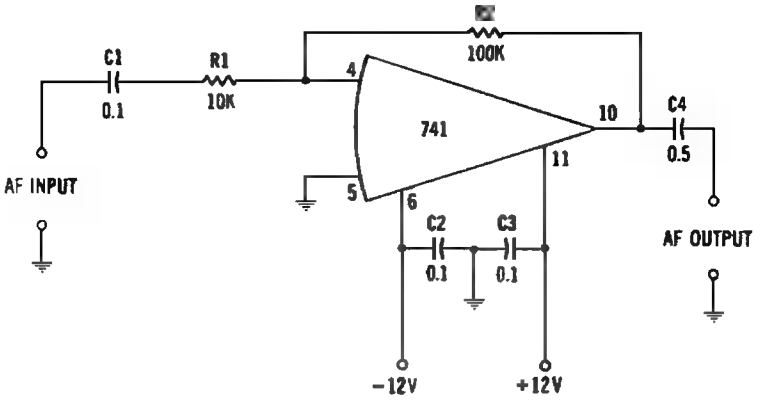


Fig. 3-2. Gain-of-10 audio amplifier.

fier or as a preamplifier where a stable amplification of 20 dB is desired.

Check the circuit for (1) dc drain, (2) maximum input-signal amplitude, (3) maximum output-voltage swing, (4) input impedance, (5) output impedance, (6) voltage gain, (7) frequency response, (8) output/input phase, and (9) total harmonic distortion.

3.3 GAIN-OF-100 AUDIO AMPLIFIER

Fig. 3-3 shows the circuit of an audio amplifier having a voltage gain of 100. Here, the gain is set by negative feedback and is deter-

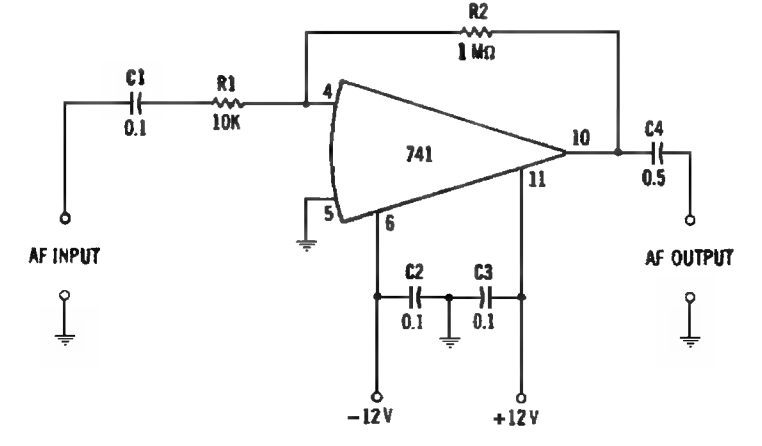


Fig. 3-3. Gain-of-100 audio amplifier.

mined by the ratio of the 1-megohm feedback resistance to the 10-kilohm input resistance ($A_v = R2/R1$). This unit is usable either as a main amplifier or as a preamplifier where a stable amplification of 40 dB is desired.

Check the circuit for (1) dc drain, (2) maximum input-signal amplitude, (3) maximum output-voltage swing, (4) input impedance, (5) output impedance, (6) frequency response, (7) voltage gain, (8) phase relationship of the input and output signals, and (9) total harmonic distortion.

3.4 GAIN-OF-1000 AUDIO AMPLIFIER

Fig. 3-4 shows the circuit of an audio amplifier having a voltage gain of 1000. Here, the gain is set by negative feedback and is determined by the ratio of the 10-megohm feedback resistance to the 10-kilohm input resistance ($A_v = R2/R1$). Because of the high gain of this amplifier, all wiring must be kept as short as practicable; this applies especially to the input circuit (C1, R1, and the ground lead from terminal 5 of the IC). This unit is usable as a sensitive main amplifier or as a preamplifier where a stable amplification of 60 dB is desired.

Check the circuit for (1) dc drain, (2) maximum input-signal amplitude, (3) maximum output-voltage swing, (4) input impedance, (5) output impedance, (6) frequency response, (7) voltage gain, (8) phase relationship of the input and output signals, and (9) total harmonic distortion.

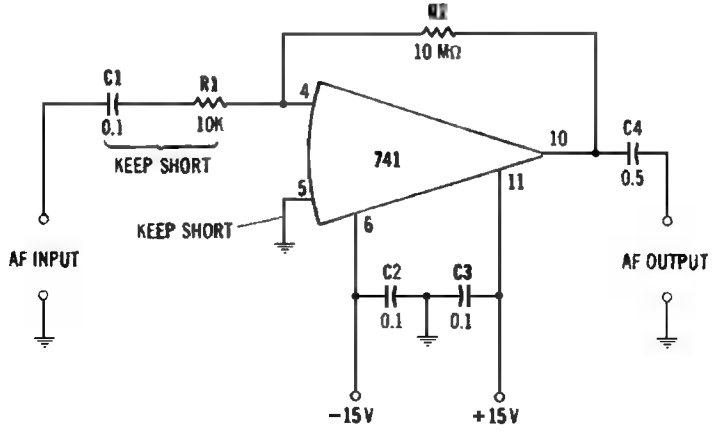


Fig. 3-4. Gain-of-1000 audio amplifier.

3.5 NONINVERTING AMPLIFIER

In the amplifiers described in Sections 3.2, 3.3, and 3.4, the output signal is out of phase with the input signal. This results from applying the input signal to the inverting input terminal of the IC. The phase reversal is not always desirable in some applications, and Fig. 3-5 shows the remedy. Here, the input signal is applied to the *noninverting* input (terminal 5 of the IC), and only the feedback is applied to the inverting input (terminal 4). The voltage gain of this amplifier is 100 (i.e., 40 dB), determined by the ratio of the 10,000-ohm resistor to the 100-ohm resistor in the negative-feedback voltage divider ($A_v = R3/R2$).

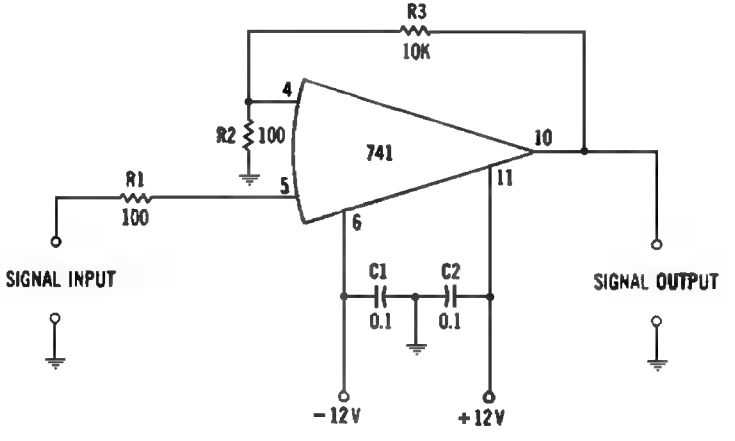


Fig. 3-5. Noninverting amplifier.

Check the circuit for (1) dc drain, (2) maximum input-signal amplitude, (3) maximum output-voltage swing, (4) input impedance, (5) output impedance, (6) frequency response, (7) voltage gain, (8) phase relationship between the input and output signals, and (9) total harmonic distortion.

3.6 LIMITER AMPLIFIER

The 54-dB gain of the circuit shown in Fig. 3-6 is useful in many applications. This amplifier receives a sine-wave input signal and delivers a clipped–sine-wave output signal; both positive and negative output-signal peaks are limited in this manner. Thus, the circuit limits, as well as amplifies. In this circuit, R3 is an offset-null potentiometer

which is set for equal clipping of the positive and negative peaks of the output signal. Output capacitor C4 is needed only when strict ac coupling is demanded. The voltage gain of the amplifier is 510, determined by the ratio of the 5.1-megohm feedback resistance to the 10,000-ohm input resistance ($A_v = R2/R1$).

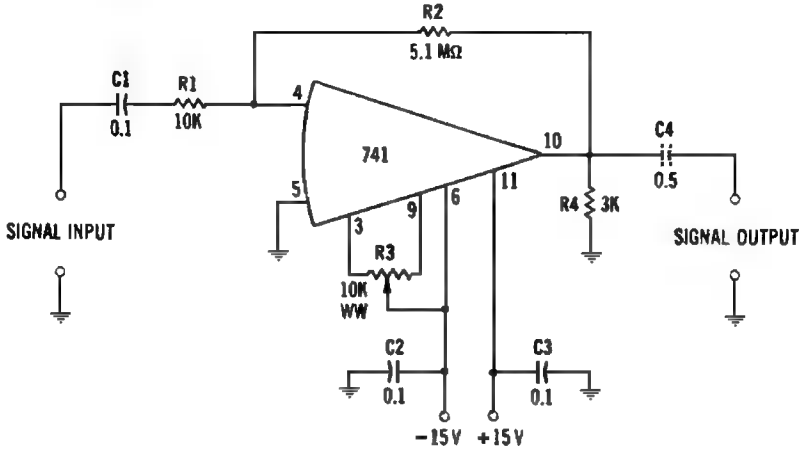


Fig. 3-6. Limiter amplifier.

Check the circuit for (1) dc drain, (2) maximum input-signal amplitude for good clipping of the output signal, (3) output-signal peak clipped voltage, (4) positive/negative symmetry in the clipped output signal, (5) input impedance, (6) frequency response, (7) voltage gain, and (8) input/output phase.

3.7 SINGLE-SUPPLY AUDIO AMPLIFIER

Fig. 3-7 shows the circuit of an audio amplifier operated from a single 12-volt dc supply. This circuit employs both negative feedback (through resistors R1 and R2) and positive feedback (through resistors R3 and R4). Potentiometer R1 also serves as a gain control for the amplifier.

Check the circuit for (1) dc drain; and *at selected settings of gain control R1*, check (2) maximum input-signal amplitude, (3) maximum output-voltage swing, (4) input impedance, (5) output impedance, (6) frequency response, (7) voltage gain, (8) phase relationship between the input signal and output signal, and (9) total harmonic distortion.

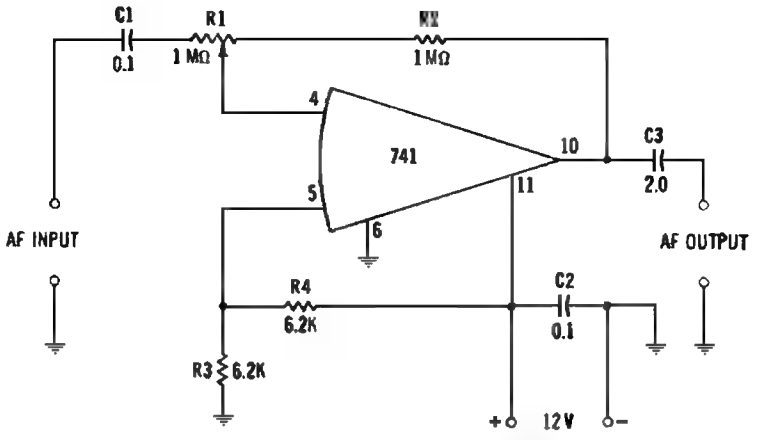


Fig. 3-7. Single-supply audio amplifier

3.8 AUDIO MIXER

Fig. 3-8 shows the circuit of a four-input audio mixer. Jacks J1 through J4 may accommodate any combination of two to four similar or dissimilar signal sources (microphones, reproducers, transducers, etc.). Any of the jacks will accommodate a single source. The voltage gain of the circuit is 10, determined by the ratio of the 510K feedback resistance to any of the 51K input resistances

Check the circuit for (1) dc drain; and for each input (J1 through J4), check (2) maximum input-signal amplitude, (3) maximum

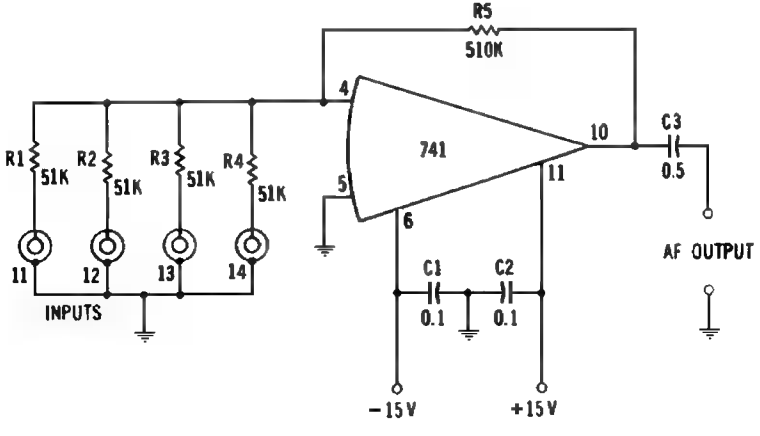


Fig. 3-8. Audio mixer.

output-voltage swing, (4) input impedance, (5) output impedance, (6) frequency response, (7) voltage gain, (8) output/input phase, and (9) total harmonic distortion. With two or more selected signals applied simultaneously to the amplifier, check the mixer action.

3.9 DC AMPLIFIER

Fig. 3-9 shows the circuit of a noninverting dc amplifier having a voltage gain of 10. The gain may be set precisely by means of trimmer potentiometer R3, and is determined by the ratio of the feedback voltage-divider resistances: (R2 + R3)/R1. If the IC has discernible zero-signal output voltage due to offset, the offset-null potentiometer, R4, may be added for adjusting this voltage to zero. (This null will be effective only over a narrow temperature range.)

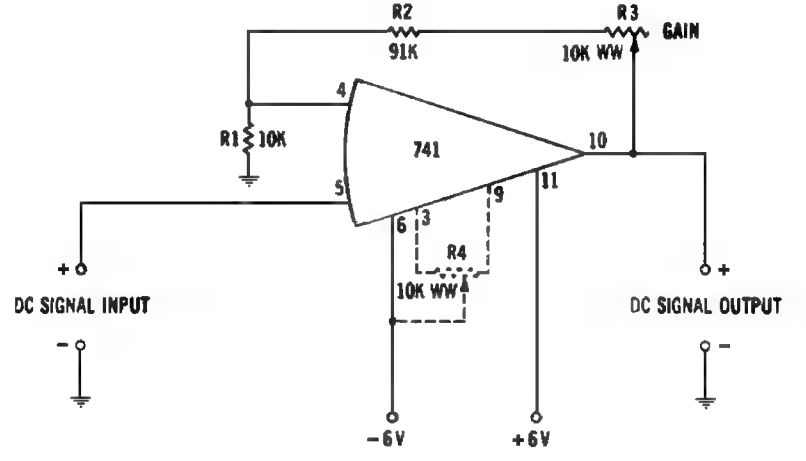


Fig. 3-9. Dc amplifier.

Check the circuit for (1) dc drain; and with gain potentiometer R3 at various selected settings, check (2) maximum input-signal voltage, (3) maximum output-voltage swing, (4) output/input linearity (5) input resistance, and (6) output resistance.

3.10 TWIN-T AUDIO OSCILLATOR

Fig. 3-10 shows the circuit of a low-distortion, 1-kHz sine-wave oscillator employing a twin-T RC null network (C1, C2, C3, R3, R4, R5) in the negative-feedback loop as the frequency-determining sec-

tion. Positive feedback is provided through the R1-R6 voltage divider and causes the circuit to oscillate. Potentiometer R6 sets the intensity of positive feedback and thus is the oscillation control.

In the twin-T network, C2 = C3 = ½C1, and R3 = R4 = 2R5.

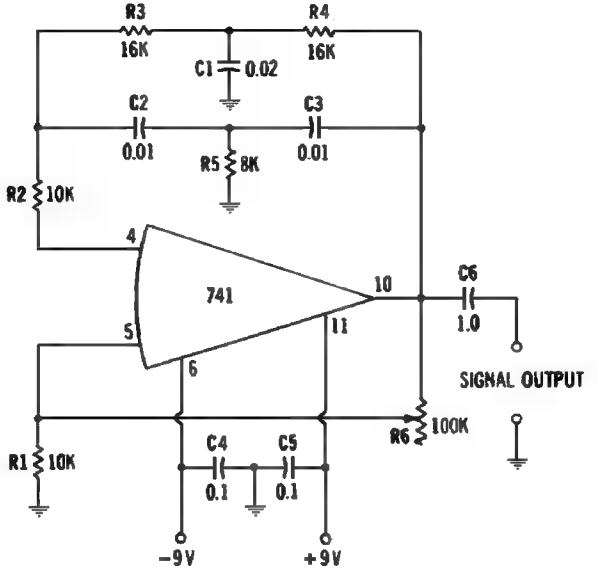


Fig. 3-10. Twin-T audio-oscillator.

The null frequency (and therefore the oscillation frequency) then is.

$$f = \frac{1}{2\pi R3C2}$$

where,

f is the frequency in hertz,
R3 is in ohms,
C2 is in farads.

The reader may use these relationships to select resistors and capacitors for other frequencies. The values given in Fig. 3-10 actually result in a frequency of 994.7 Hz. For exactly 1000 Hz, trim resistors R3 and R4 to 15,915 ohms, and R5 to 7957 ohms. (It is easier to prune resistance than high capacitance.)

Check the circuit for (1) dc drain, (2) signal-output voltage, (3) signal frequency, and (4) total harmonic distortion (adjust R6 for lowest distortion and easiest starting of oscillation).

3.11 WIEN-BRIDGE AUDIO OSCILLATOR

The low-distortion, 1-kHz sine-wave oscillator shown in Fig. 3-11 employs only four components (C1, C2, R1, R2) in its RC-type frequency-determining network, compared with the previous oscillator (Fig. 3-10) which requires six. In Fig. 3-11, C1, C2, R1, and R2 form a Wien bridge in which C1 = C2, and R1 = R2. The oscillation frequency then is:

$$f = \frac{1}{2\pi R1C1}$$

where,

f is the frequency in hertz,
R1 is in ohms,
C1 is in farads.

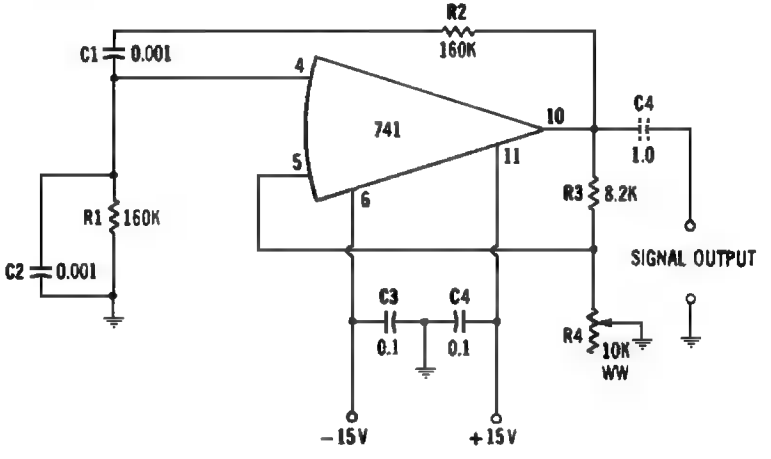


Fig. 3-11. Wien-bridge audio oscillator.

The reader may use these relationships to select resistors and capacitors for other frequencies. The values given in Fig. 3-11 actually result in a frequency of 994.7 Hz. For exactly 1000 Hz, trim resistors R1 and R2 to exactly 159,155 ohms. (It is easier to prune resistance than high capacitance.) Output capacitance C4 is needed only for strict ac coupling.

Check the circuit for (1) dc drain, (2) output-signal voltage, (3) signal frequency, and (4) total harmonic distortion (adjust R4 for lowest distortion and easiest starting of oscillation).

3.12 ASTABLE MULTIVIBRATOR

Fig. 3-12 shows the circuit of an astable (free-running) multivibrator which will deliver a 1-kHz square-wave output. The frequency is determined by the time constant of the R1-C1 combination. The circuit operates from a single 5-volt dc supply.

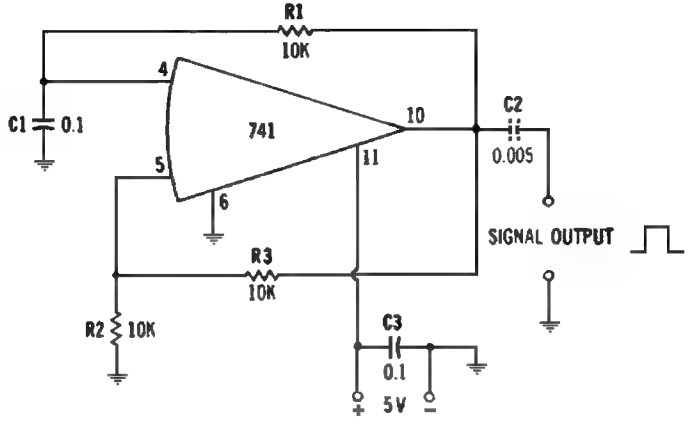


Fig. 3-12. Astable multivibrator.

Increase either R1 or C1 to lower the frequency; decrease either one to increase the frequency. With an individual IC, changing the ratio of resistance R3 to resistance R2 may improve the output waveform and amplitude. Output capacitor C2 is needed only for strict ac coupling.

Check the circuit for (1) dc drain, (2) output-signal voltage, (3) squareness of output signal, and (4) signal frequency.

3.13 LOW-PASS FILTER

Fig. 3-13 shows the circuit of an active low-pass filter of the Sallen-Key type, having a cutoff frequency of 1000 Hz. In this type of circuit, positive feedback introduced into the RC filter section (R1, R2, C1, C2) by the integrated circuit sharpens the filter response.

The values of C1, C2, R1, R2, R3, and R4 must be held as close as possible. Resistances R1, R2, and R3 each may be composed of 15,000 ohms and 915 ohms in series; R4 may be 10,000 ohms and 820 ohms in series. (It is easier to prune resistance than high capacitance.)

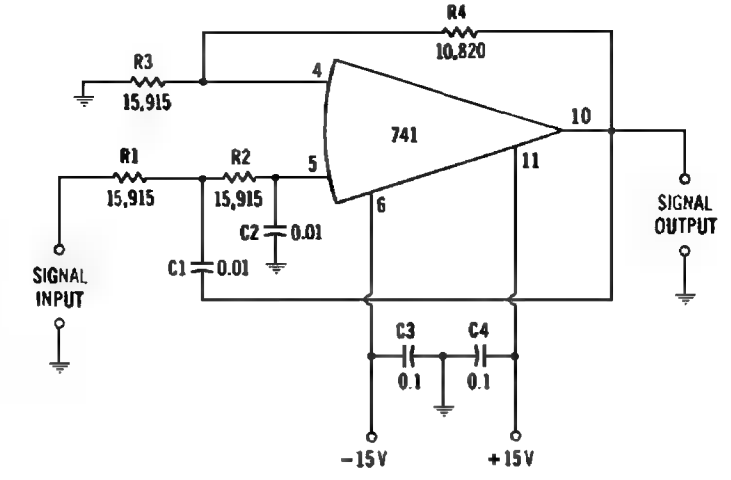


Fig. 3-13. Low-pass filter.

Check the circuit for (1) dc drain, (2) frequency response, (3) maximum input-signal amplitude, (4) maximum output-voltage swing, and (5) voltage gain in the passband.

3.14 HIGH-PASS FILTER

Fig. 3-14 shows the circuit of an active high-pass filter of the Sallen-Key type, having a cutoff frequency of 1000 Hz. In this type of circuit, positive feedback introduced into the RC filter section (R1, R2, C1, C2) by the integrated circuit sharpens the filter response.

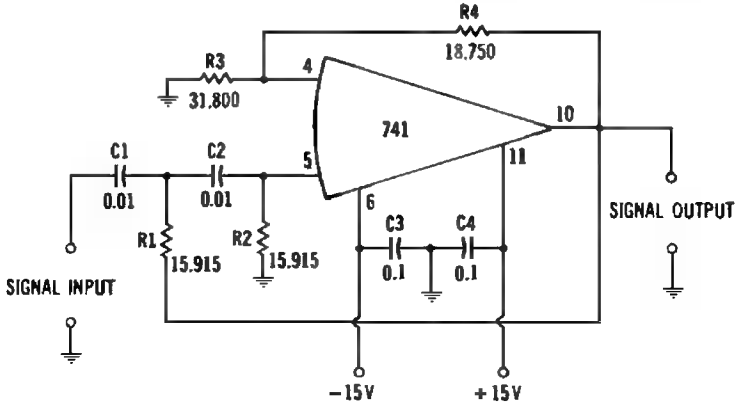


Fig. 3-14. High-pass filter.

The values of C1, C2, R1, R2, R3, and R4 must be held as close as possible. Resistances R1 and R2 each may be composed of 15,000 ohms and 915 ohms in series, R3 may be 30,000 ohms and 1800 ohms in series, and R4 may be 18,000 ohms and 750 ohms in series. (It is easier to prune resistance than high capacitance.)

Check the circuit for (1) dc drain, (2) frequency response, (3) maximum input-signal amplitude, (4) maximum output-voltage swing, and (5) voltage gain.

3.15 BANDPASS FILTER (TYPE 1)

The 1-kHz active bandpass filter shown in Fig. 3-15 employs a twin-T RC null network (R2, R3, R4, C2, C3, C4) in the negative-feedback loop to determine the center frequency of the passband of

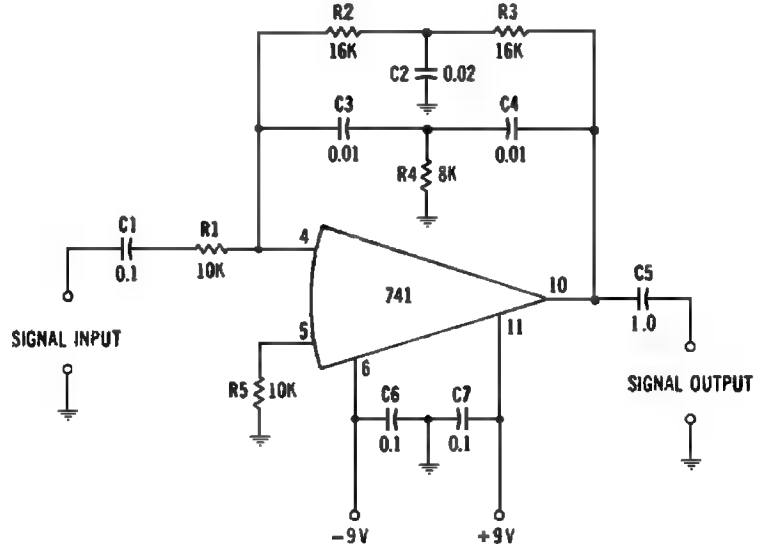


Fig. 3-15. Bandpass filter (Type 1)

the filter. Because this network removes one frequency (actually a narrow band of frequencies) from the fed-back energy, that frequency is transmitted by the IC amplifier, and all others are reduced or nulled. In the twin-T network, C3 = C4 = ½C2, and R2 = R3 = 2R4. Under these conditions, the null frequency (and therefore the center frequency of the passband) then is:

$$f = \frac{1}{2\pi R2C3}$$

where,

f is the frequency in hertz,
R2 is in ohms,
C3 is in farads.

The reader may use these relationships to select resistors and capacitors for other frequencies. The values given in Fig. 3-15 actually result in a frequency of 994.7 Hz. For exactly 1000 Hz, trim resistors R2 and R3 to 15,915 ohms, and R4 to 7957 ohms. (It is easier to prune resistance than high capacitance.)

Check the circuit for (1) dc drain, (2) frequency response, (3) maximum input-signal amplitude, (4) maximum output-voltage swing, and (5) voltage gain.

3.16 BANDPASS FILTER (TYPE 2)

Fig. 3-16 shows the circuit of a 1-kHz active bandpass filter of the multiple-feedback type, so called from the dual feedback path pro-

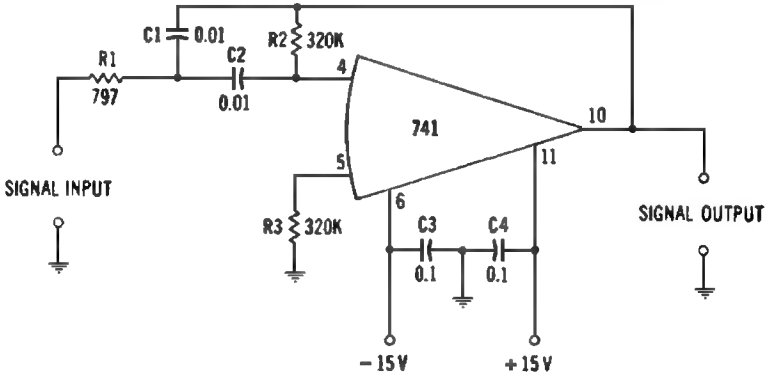


Fig. 3-16. Bandpass filter (Type 2).

vided by C1 and R2. In this circuit, the frequency-determining resistances and capacitances (R1, R2, R3, C1, C2) must be held as close as possible. Resistance R1 may be 750 ohms and 47 ohms in series, and R2 and R3 each may be 300K and 20K in series. When C1 = C2 = 0.01 μF and a filter Q of 10 is acceptable, for any frequency f in hertz, R1 = 795,800/f, and R2 = R3 = 400R1.

Check the circuit for (1) dc drain, (2) frequency response, (3) maximum input-signal amplitude, (4) maximum output-voltage swing, and (5) voltage gain. Compare the performance of this filter with the performance of the Type-1 unit described in Section 3.15.

3.17 HIGH-Q NOTCH FILTER

Use of the twin-T notch filter is widespread in electronics. This filter rejects one frequency (actually a narrow band of frequencies); however, its null is not always as deep nor its bandwidth as narrow as might be desired. This is the result of the comparatively low Q of the RC circuit. In Fig. 3-17, the IC in conjunction with the twin T (R1, R2, R3, C1, C2, C3) sharpens the network response (boosts its Q) by introducing positive feedback at the junction of C1 and R3 and by lightly loading the twin T. Here, the IC functions as a voltage follower by reason of the 100-percent negative feedback provided by the solid path between output terminal 10 and inverting-input terminal 4.

In the twin-T network, $C2 = C3 = \frac{1}{2}C1$, and $R1 = R2 = 2R3$. The notch frequency is:

$$f = \frac{1}{2\pi R1C2}$$

where,

f is the frequency in hertz,
R1 is in ohms,
C2 is in farads.

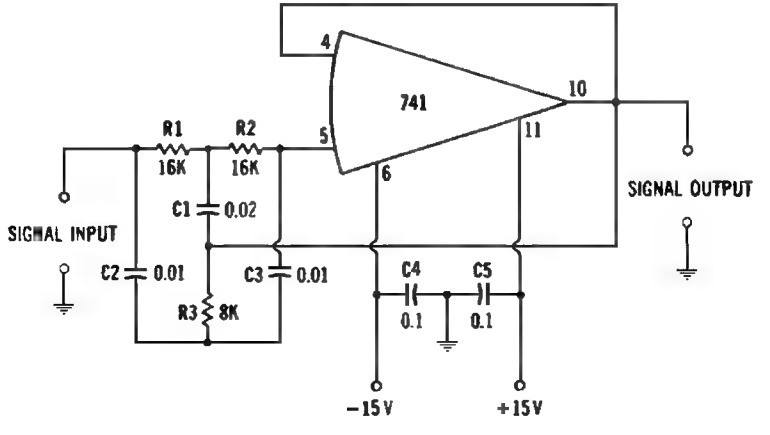


Fig. 3-17. High-Q notch filter.

The values given in Fig. 3-17 actually result in a frequency of 994.7 Hz. For exactly 1000 Hz, trim resistors R1 and R2 to 15,915 ohms, and R3 to 7957 ohms. (It is easier to prune resistance than high capacitance.)

Check the circuit for (1) dc drain, (2) frequency response, (3) maximum input-signal amplitude, (4) maximum output-voltage swing, and (5) voltage gain.

3.18 DIFFERENTIATOR

Fig. 3-18 shows the circuit of an active differentiator. The relationship between the input and output voltages in this circuit is given by the expression $E_{out} = (dE_{in}/dt)R1C1$. Thus, the output is proportional to the differential of the input; and for a square-wave input signal, as shown in Fig. 3-18, the output is a sharp spike. Similarly, under ideal conditions, a cosine-wave output results from a sine-wave input. The circuit is entirely straightforward; with some ICs, however, and at some frequencies, inclusion of resistor R2 may be helpful.

Check the circuit for (1) dc drain, (2) output waveform obtained with square-wave input, and (3) output waveform obtained with sine-wave input. Repeat Steps 2 and 3 at several selected frequencies.

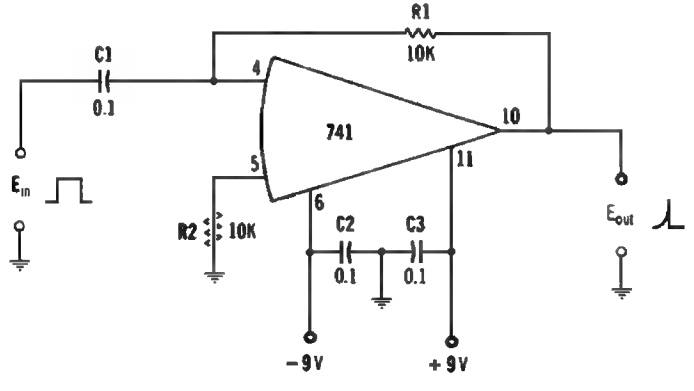


Fig. 3-18. Differentiator.

3.19 INTEGRATOR

Fig. 3-19 shows the circuit of an active integrator. The relationship between input and output voltages in this circuit is given by the ex-

pression $E_{out} = -(1/R1C1) \int E_{in}\, dt$. Thus, the output is proportional to the integral of the input; and for a square-wave input, as shown in Fig. 3-19, the output is a sawtooth. Similarly, under ideal conditions, a sine-wave output results from a cosine-wave input. As with the differentiator previously described, the circuit is entirely straightforward; however, with some ICs and at some frequencies, inclusion of resistor R2 may be helpful.

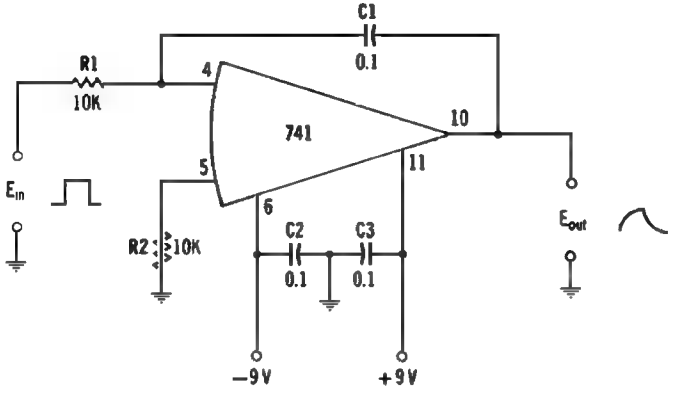


Fig. 3-19. Integrator.

Check the circuit for (1) dc drain, (2) output-signal waveform obtained with square-wave input, and (3) output-signal waveform obtained with sine-wave input. Repeat Steps 2 and 3 at several selected frequencies.

3.20 PRECISION RECTIFIER

A unique, precision half-wave rectifier is shown in Fig. 3-20. This circuit overcomes three of the frustrating peculiarities of the semiconductor diode: nonlinearity, temperature drift, and the threshold at which rectification starts. In Fig. 3-20, the IC functions as a unity-gain voltage follower with diode D1 in the feedback loop. Since feedback thus can take place only during the conduction half-cycle, when D1 is forward biased, the follower operates only during this half-cycle, delivering a positive half-cycle of voltage at the dc-output terminals. During the positive half-cycle of the ac input voltage, the IC switches off (this being an inverting amplifier), since D1 then cannot conduct. Diode D2 (identical to D1) clamps the IC when the latter is in this off state, and this prevents saturation and allows the diode

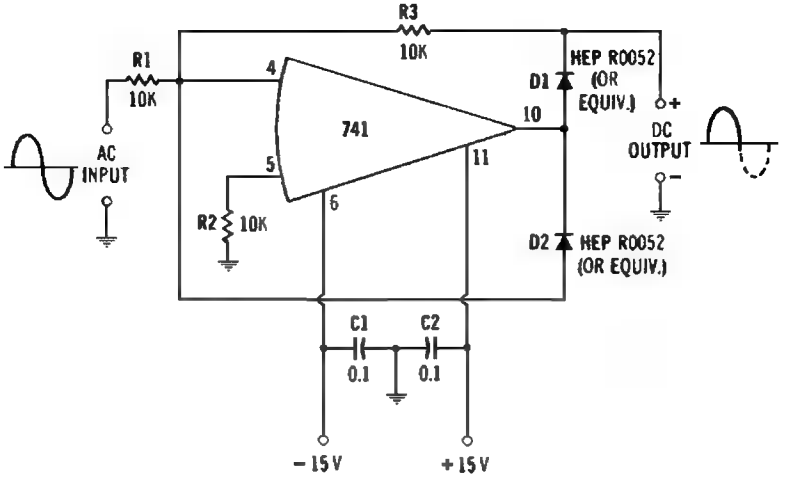


Fig. 3-20. Precision rectifier.

to operate at higher frequencies than it otherwise might reach. For efficient operation of the circuit, resistors R1 and R3 must be matched within 1 percent.

Check the circuit for (1) dc drain, (2) output waveform and amplitude for various selected frequencies of sine-wave input voltage, and (3) linearity as shown by the relationship between the output and input voltages at several selected steps of input voltage. (4) Reverse both D1 and D2 for negative output, and repeat Steps 1 through 3.

3.21 ANALOG ADDER

Fig. 3-21 shows the circuit of a gain-of-1 dc amplifier and inverter adapted for analog addition. Here, the output voltage, E_{out}, equals the sum of any number of positive input voltages up to the maximum allowable output-voltage swing of the IC, 10 volts. Thus, $E_{out} = -(E1 + E2 + E3 + E4 + \ldots E_n)$. The unity gain of the device is determined by the 1:1 ratio of feedback resistance R5 to input resistance R1 (or R2 . . . R_n). The inversion (sign change) results from application of the quantities to be summed to the inverting input (terminal 4) of the IC.

Check the circuit for (1) dc drain and (2) maximum output-voltage swing when the input test voltage is applied to one of the input terminals. (3) Check the adding function: Apply known voltages

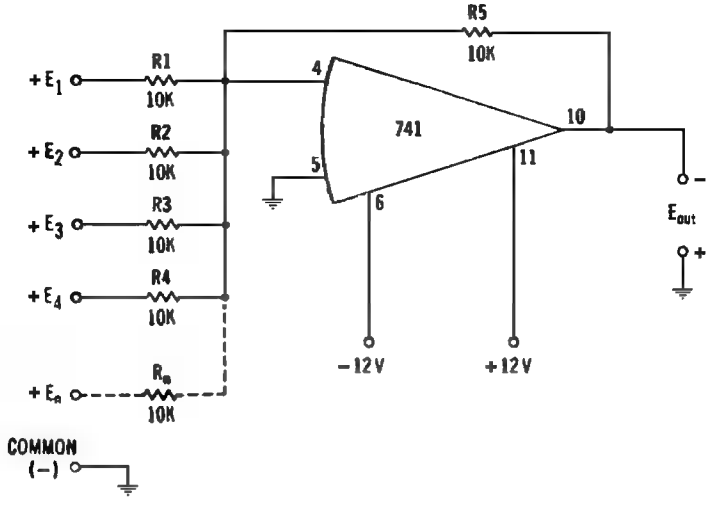


Fig. 3-21. Analog adder.

to selected input terminals, and note the sum voltage at the E_{out} terminals.

3.22 MILLIAMMETER WITH LOW INPUT RESISTANCE

Fig. 3-22 shows the circuit of an electronic dc milliammeter having an input resistance of only 10 ohms. The low input resistance (set by

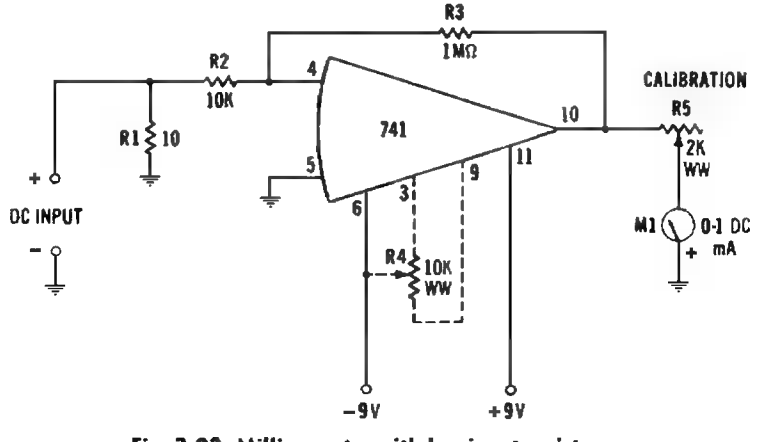


Fig. 3-22. Milliammeter with low input resistance.

resistor R1) results in very low voltage drop across the instrument when it is inserted into a circuit. In this arrangement, the IC acts as a dc amplifier (A_v = approximately 100) ahead of a 0–1 dc milliammeter, M1. (When the meter is inserted directly into a circuit to measure current, it introduces a resistance of 50 to 100 ohms, depending upon make and model.) The zero-setting potentiometer, R4, will be required only if the offset of the 741 is high enough to deflect meter M1 when no signal is present at the dc-input terminals.

To check the circuit: (1) Apply an accurately known current of 1 mA to the dc-input terminals. (2) Adjust calibration control potentiometer R5 for exact full-scale deflection of meter M1. (3) Test for linearity by setting the input signal to selected current levels between zero and 1 mA and observing the corresponding deflections of meter M1. (4) Check the dc drain at (a) zero-signal and (b) maximum-signal input. (5) If equipment is available, check the setup for temperature drift.

As it is shown here, the circuit is satisfactory for 0–1 mA input. For other current ranges, change the value of R1. Thus, for 0–10 mA, R1 = 1 ohm; for 0–100 mA, R1 = 0.1 ohm. That is, $R_x = R1/I = 10/I$, where R_x = required resistance (ohms) and I = desired full-scale deflection (mA).

3.23 ELECTRONIC DC MICROAMMETER

In the circuit shown in Fig. 3-23, a dc amplifier converts 0–1 dc milliammeter M1, a relatively rugged instrument, into a microam-

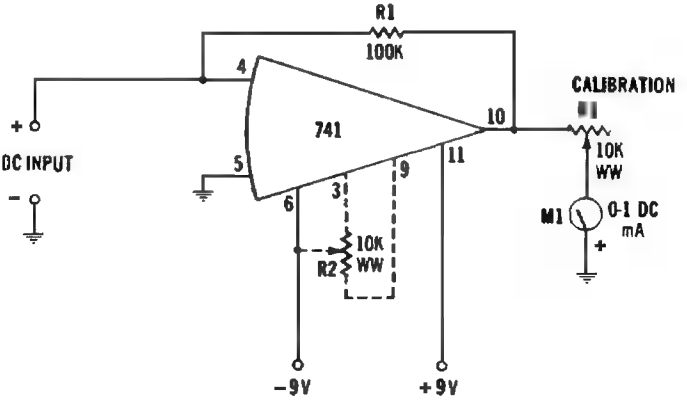


Fig. 3-23. Electronic dc microammeter.

meter with full-scale deflection of approximately 1 μA. The zero-setting potentiometer, R2, will be required only if the offset of the 741 is high enough to deflect meter M1 when no signal is present at the dc-input terminals.

To check the circuit: (1) Apply an accurately known current of 1 μA to the dc-input terminals. (2) Adjust calibration control potentiometer R3 for exact full-scale deflection of meter M1. (3) Test for linearity by setting the input signal to selected current levels between zero and 1 μA and observing the corresponding deflections of meter M1. (4) Check the dc drain at (a) zero-signal and (b) maximum-signal input. (5) If equipment is available, check the setup for temperature drift.

As it is shown here, the circuit is satisfactory for 0–1 μA input For other current ranges, switch in additional R3 potentiometers in place of the 10K value. Determine experimentally the potentiometer resistance setting for each desired current range.

3.24 ELECTRONIC DC MILLIVOLTMETER

Fig. 3-24 shows the circuit of a 0–10 dc millivoltmeter consisting of an IC dc amplifier and a 0–1 dc milliammeter (M1). This instrument will serve in applications where a dc millivoltmeter having reasonably high input resistance is needed (see, for example, Experiments 5, 6, and 25 in Part 2 of this book). If the offset of the 741 is high enough to deflect meter M1 when no signal is present at the

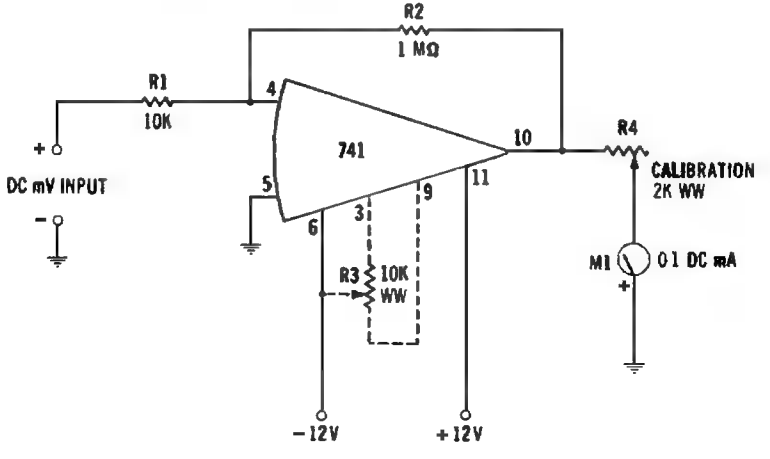


Fig. 3-24. Electronic dc millivoltmeter.

dc input terminals, use potentiometer R3 for zero setting. The dc gain of the setup is approximately 100, determined by the ratio of R2 to R1.

To check the circuit: (1) Apply an accurately known voltage of 10 mV to the dc-input terminals. (2) Adjust calibration control potentiometer R4 for exact full-scale deflection of meter M1. (3) Test for linearity by setting the input signal to selected voltage levels between zero and 10 mV and observing the corresponding deflections of meter M1. (4) Check the dc drain at (a) zero-signal and (b) maximum-signal input. (5) If equipment is available, check the setup for temperature drift.

As it is shown here, the circuit is satisfactory for 0–10 mV input. For other millivolt ranges, switch in additional R4 potentiometers. Determine experimentally the potentiometer resistance setting for each desired range.

3.25 ELECTRONIC DC VOLTMETER

Fig. 3-25 shows an IC version of an old favorite among basic test instruments, the electronic dc voltmeter. Like its predecessors, the vacuum-tube voltmeter, transistor voltmeter, and FET voltmeter, this instrument offers high input resistance (10 megohms) and a balanced input circuit. In this setup, the integrated circuit (741) operates as a high–input-resistance dc amplifier ahead of a 0–1 dc milliammeter

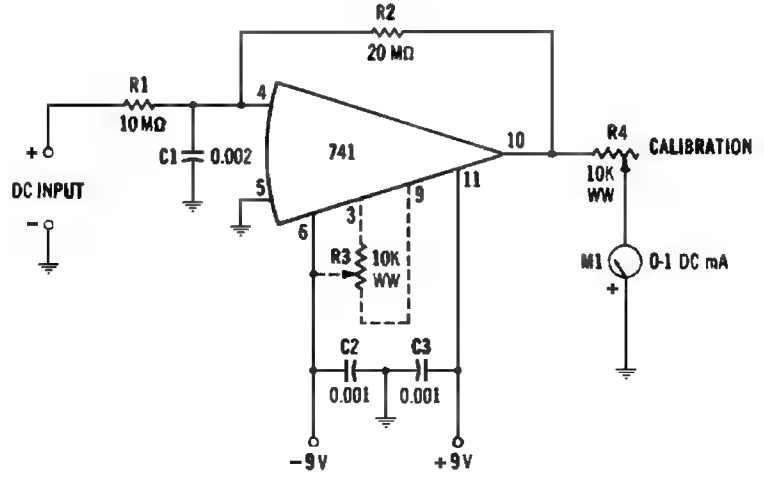


Fig. 3-25. Electronic dc voltmeter.

(M1). A potential of 1 V applied to the dc-input terminals deflects the meter to 1 mA. In many ICs, the offset voltage is so low that no zero set of the meter is necessary; with others having offset high enough to deflect the meter initially, the zero-set potentiometer, R3, may be added. Capacitor C1 in conjunction with input resistor R1 acts as a filter to reduce the effects of stray pickup. Similarly, capacitors C2 and C3 shunting the dc supplies serve to smooth out fluctuations caused by noise.

To check the circuit: (1) Apply an accurately known voltage of 1 V to the dc input terminals. (2) Adjust calibration control potentiometer R4 for exact full-scale deflection of meter M1. (3) Test for linearity by setting the input signal to selected voltage levels between zero and 1 V and observing the corresponding deflections of meter M1. (4) Check the dc drain at (a) zero-signal and (b) 1-V dc input. (5) If equipment is available, check the setup for temperature drift.

As it is shown here, the circuit is satisfactory for 0–1 V input. For other voltage ranges, a suitable voltage divider may be used to reduce those voltages to 1 V. In this way, meter M1 may be made to indicate zero to 1, 10, 100, or 1000 V.

3.26 LOGARITHMIC CONVERTER

The specialized dc amplifier setup shown in Fig. 3-26 converts a linear dc input into an approximately logarithmic dc output. In this arrangement, a silicon bipolar transistor (Q1) is inserted into the negative-feedback loop, and the logarithmic response of this transistor

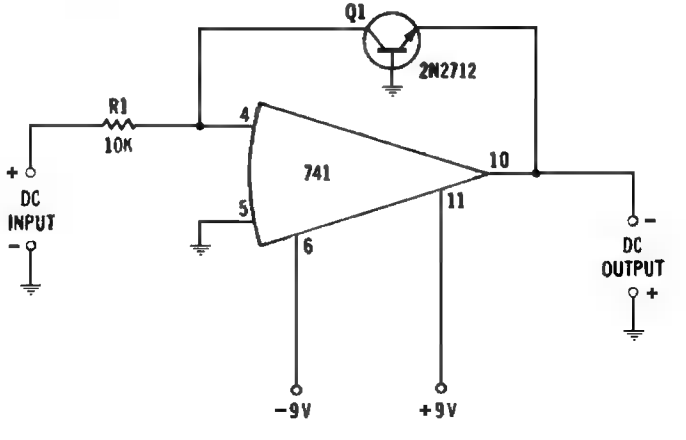


Fig. 3-26. Logarithmic converter.

over a portion of its operating range is imparted to the IC. This type of converter finds application in instrumentation, control, analog calculating, and signal processing.

To check the circuit: (1) Starting with 0.05 V, apply a selected series of accurately known dc voltages in linear steps to the dc-input terminals. (2) Observe the corresponding dc output voltages. (3) Plot output voltage against input voltage, and note from the graph the range over which E_{output} varies logarithmically as E_{input} varies linearly. In this region, the output voltage changes rapidly as the input voltage changes slowly. (4) If components are available, repeat Steps 1 through 3 with different 2N2712 transistors (Q1) in the circuit. (5) Check the dc drain at (a) zero dc signal input and (b) maximum dc signal input at which circuit response is still logarithmic. (6) If equipment is available, check the setup for temperature drift.

3.27 SENSITIVE LIGHT METER

An integrated-circuit dc amplifier between a self-generating silicon photocell and a dc milliammeter, as shown in Fig. 3-27, boosts the performance of the conventional light-meter circuit (cell plus meter). With this arrangement, very low light intensity will give full-scale deflection of the 0–1 dc milliammeter, M1 (a comparatively rugged meter when compared with the sensitive microammeter required in the rudimentary circuit). The silicon cell, PC, is Type S1M-C or equivalent. In many ICs, the offset voltage is so low that no darkened-cell zero set of the meter is necessary; with others having offset

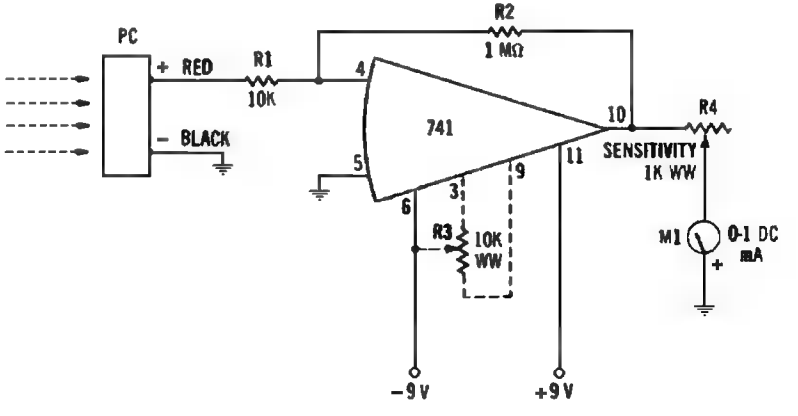


Fig. 3-27. Sensitive light meter.

high enough to deflect the meter, the zero-set potentiometer, R3, may be added.

To check the circuit: (1) With calibration control potentiometer R4 set arbitrarily to center range, illuminate photocell PC, noting that meter M1 deflects upscale. (2) If a light source of accurately known intensity is available, use it to illuminate the cell steadily, and set potentiometer R4 for exact full-scale deflection of the meter. (3) Vary the intensity of the light source, while keeping constant the distance between source and cell, and note the corresponding deflections of the meter. (4) Check the dc drain with (a) the cell completely darkened, and (b) the cell receiving maximum illumination.

For separate ranges of the instrument, experimentally determined values of either R2 or R4 may be switched into the circuit. Increasing R2 increases the sensitivity; increasing R4 decreases the sensitivity.

3.28 ELECTRONIC THERMOMETER

Fig. 3-28 shows the circuit of an electronic temperature-sensing device which may be employed either as a thermometer or as a temperature control. The temperature sensor is a thermistor, R1, which may be located remotely, if desired.

In this arrangement, the thermistor is connected in a 4-arm bridge (R1, R2, R3, R4) which is balanced for zero output at room temperature or any other desired reference temperature. A change in temperature above or below this reference value unbalances the bridge through the change in thermistor resistance, and the resulting

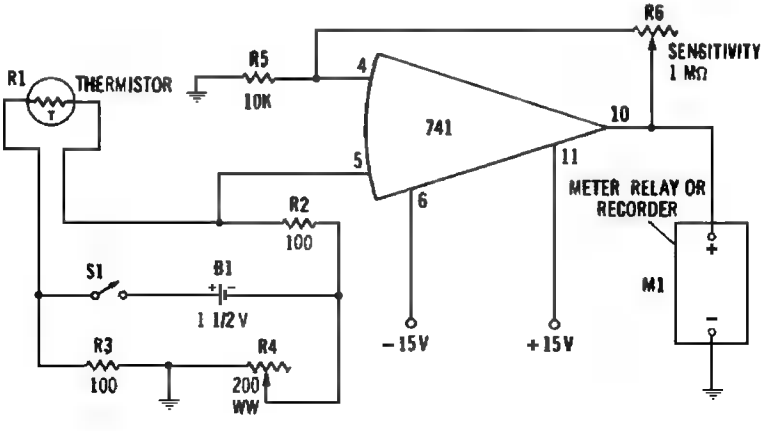


Fig. 3-28. Electronic thermometer.

dc output is applied to the IC, which acts as a dc amplifier. The dc output of the amplifier then drives M1, which may be a milliammeter, milliampere-type dc relay, or direct-writing recorder.

Check the circuit in the following manner: (1) At the reference temperature, note the amplifier output indicated by M1. (2) Close switch S1, and adjust potentiometer R4 to zero-set M1 to the desired level corresponding to this temperature. (3) Expose the thermistor to a new temperature, and observe the deflection of M1. (4) To change the sensitivity of the circuit, adjust potentiometer R6, and repeat Steps 1, 2, and 3. (5) If M1 is a relay, it may be adapted either to open or close a circuit in response to a given temperature change. (6) Check the dc drain at the minimum and maximum temperatures.

3.29 ANALOG-TYPE AUDIO FREQUENCY METER

Fig. 3-29 shows the circuit of a direct-reading audio frequency meter. In this setup, the 0–100 dc microammeter, M1, reads 0–10,000 Hz and gives linear response so that only the top point (100 μA, 10 kHz) need be calibrated. The basis of this instrument is a squarer consisting of the 741 IC with a zener diode (D1) in its negative-feedback loop. This arrangement delivers constant-amplitude square waves to the metering circuit (C3, D2, D3, M1, R2), so the deflection of microammeter M1 is proportional only to the frequency. Operation is independent of the amplitude and waveform of the signal applied to the af-input terminals, over a wide range.

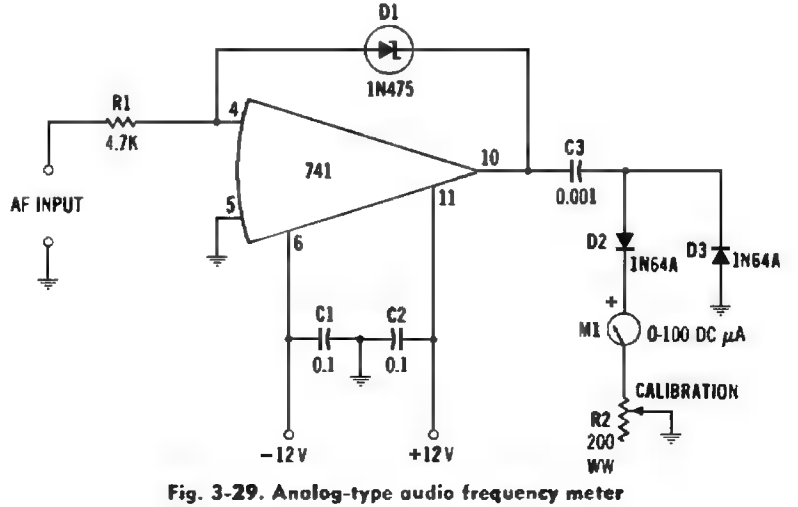


Fig. 3-29. Analog-type audio frequency meter

To check the circuit: (1) Apply a 10,000-Hz signal to the af-input terminals. (2) Set potentiometer R2 for exact full-scale deflection of meter M1. (3) Check the linearity by setting the input-signal frequency successively to 8 kHz, 7 kHz, 5 kHz, 2 kHz, and 1 kHz (the meter deflections should be 80, 70, 50, 20, and 10 μA, respectively). (4) At a selected steady frequency, vary the input-signal amplitude and change its waveform (e.g., from sine to square), and observe any change in the meter reading. (5) Check the dc drain at (a) zero and (b) maximum input-signal amplitude.

The full-scale frequency may be changed, if desired, to 0–100, 0–1000, or 0–100,000 Hz by appropriately changing the values of C3 and R2.

3.30 SOUND-LEVEL METER

A simple sound-level meter circuit is shown in Fig. 3-30. In this arrangement, the sound is picked up with a miniature crystal-microphone cartridge (mic) and is amplified by the 741 integrated circuit. A source follower (field-effect transistor Q1) transforms

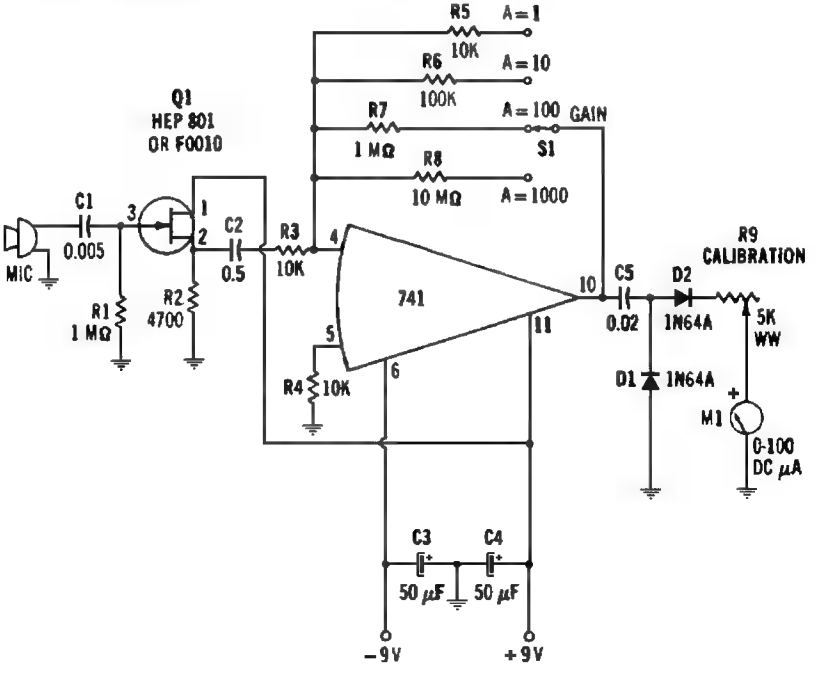


Fig. 3-30. Sound-level meter.

the high impedance of the microphone to the lower input impedance of the IC. The amplifier has four fixed levels of voltage gain ($A_v = 1$, $A_v = 10$, $A_v = 100$, and $A_v = 1000$) set by switched-in feedback resistors R5, R6, R7, and R8. The output of the amplifier drives the rectifier-type meter circuit (C5, D1, D2, R9, M1).

Check the circuit in the following manner: (1) With switch S1 at its A = 1 position, apply steady sound of known intensity to the microphone, and adjust calibration control potentiometer R9 for exact full-scale deflection of meter M1. (2) Throw switch S1 successively to its other positions, noting the deflection on each range. (3) If the sound intensity can be varied, set it to other levels, and observe the meter reading in each gain range. (4) If an accurate sound-calibration source is available, the circuit may be calibrated in decibels. (5) Check the dc drain with (a) zero sound input and (b) maximum sound input.

3.31 ELECTROSCOPE

An electroscope is convenient for detecting static electricity and also for "sniffing" high voltage without actually making contact with dangerous circuitry. The polished ball which constitutes the probe of

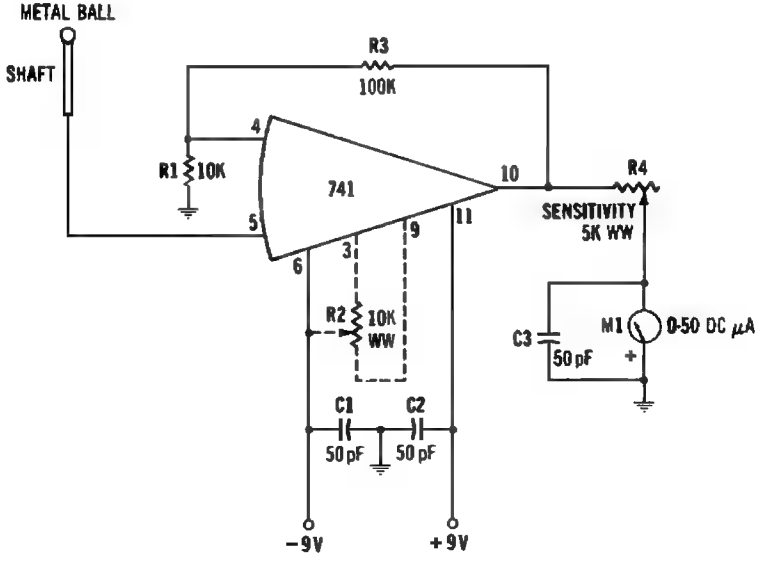


Fig. 3-31. Electroscope.

the electroscope is simply poked into the field. (This must be done with extreme caution to avoid contact with the conductors carrying the high voltage.) Fig. 3-31 shows an electroscope circuit.

In this arrangement, the pickup ball-probe is connected directly to the noninverting input of the IC. The shaft of the probe is mounted directly to, but insulated from, the case of the instrument, which can be made small enough to be handled with self-contained small batteries. The IC acts as a dc amplifier which deflects the 0–50 dc microammeter, M1, in proportion to the strength of the field into which the ball is inserted. In many ICs, the offset will not erroneously deflect the meter; but when the offset is high, potentiometer R2 may be added for zero setting of the meter.

To check the circuit: (1) Bring a charged source close to the pickup ball (a piece of paper stroked with a rod of insulating material will do). (2) Note the deflection of meter M1, and adjust sensitivity control potentiometer R4 for higher or lower deflection, as desired. (3) Position the ball near (but not touching) the high-voltage circuitry of a tv receiver, and observe the meter reading. (4) Check the dc drain with (a) zero input (no external pickup) and (b) maximum input (full pickup).

3.32 SENSITIVE DC RELAY

Fig. 3-32 shows the circuit of a relay which operates on 100 millivolts or lower at a few microamperes—a power input of only a few microwatts. In this arrangement, the dc control signal is applied to the IC operated as a gain-of-10 dc amplifier. The output of the IC drives a 1-mA, 1000-ohm dc relay, RY (Sigma 5F or equivalent). The gain of the amplifier is determined by negative feedback which, in turn, is set by the ratio of R2 to R1 in the feedback loop. The 100K potentiometer, R2, thus serves as the sensitivity control. Diode D1 protects the IC from the high-voltage inductive kickback resulting from sudden switch-off of the relay. Through proper selection of the output terminals of relay RY, this circuit may either open or close an external circuit, as desired, upon application of the control voltage. The reverse is also true: the external circuit may be either opened or closed, as desired, by interruption of the control voltage.

To check the circuit: (1) With sensitivity control potentiometer R2 set to zero, apply an adjustable dc control voltage to the dc input terminals. (2) Increase the control voltage to the desired switching value. (3) Adjust potentiometer R2 to the point at which relay RY

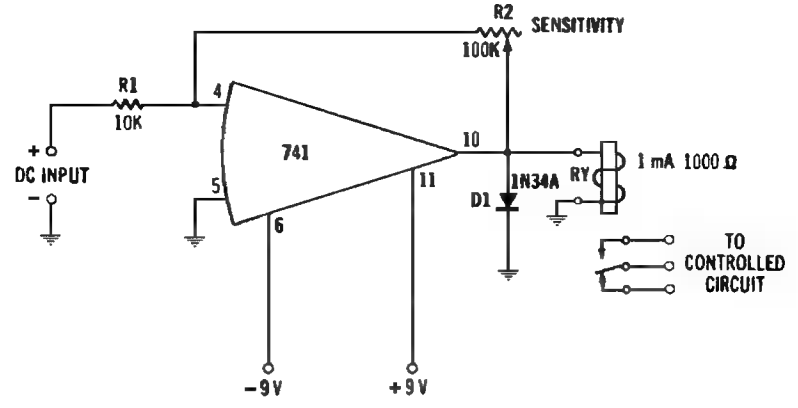


Fig. 3-32. Sensitive dc relay.

just closes. (4) At this point, measure the control-signal current at the dc input terminals. (5) Check the dc drain at (a) zero-signal input (relay open) and (b) maximum-signal input (relay closed).

3.33 SENSITIVE AF/RF RELAY

An audio- or radio-frequency signal applied to the input terminals of the circuit in Fig. 3-33 is rectified by the shunt-diode section (C1, D1, R1), and the resulting dc is applied to the 741 IC which, acting as a dc amplifier, drives the small relay, RY. The latter is a 1-mA, 1000-ohm dc unit (Sigma 5F or equivalent). so that only a tenth of

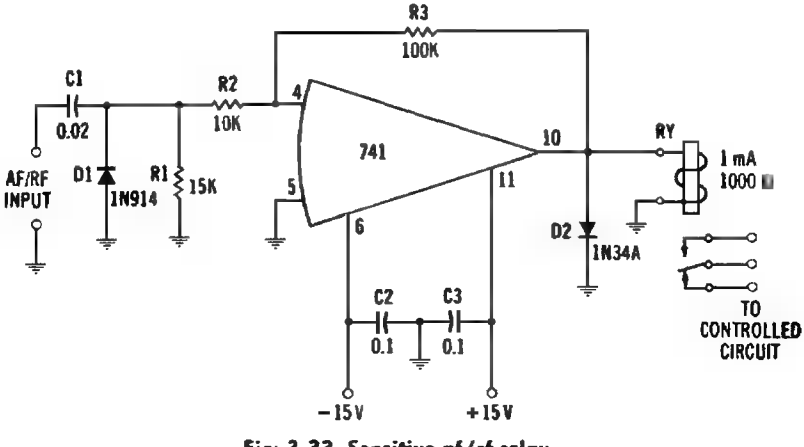


Fig. 3-33. Sensitive af/rf relay.

a volt or so is required at the af/rf input terminals to close the relay. Diode D2 protects the IC from the high-voltage inductive kick resulting from sudden switch-off of the relay.

To check the circuit: (1) Apply an adjustable af or rf voltage to the af/rf input terminals. (2) Increase the voltage to the point at which the relay just closes. (3) At this point, read the ac input voltage and (if an ac microammeter is available) the ac input current. (4) Repeat Steps 1, 2, and 3 at selected frequencies. (5) Check the dc drain at (a) zero ac-signal input and (b) the point of relay closure.

3.34 TUNED AC RELAY

Fig. 3-34 shows the circuit of an electronic relay that is tuned to approximately 1 kHz. This circuit receives its selectivity from use of the IC in a multiple-feedback active bandpass filter. For explanatory details of the latter, see Section 3.16 and Fig. 3-16. The other active bandpass filter, described in Section 3.15, also may be employed in this relay circuit. Both of the referenced sections explain how to tune the filter to frequencies other than 1 kHz. The output of the filter is rectified by the diode section (C5, D1, D2, R4), and the resulting dc is applied to relay RY, a 1-mA, 1000-ohm unit (Sigma 5F or equivalent). Capacitor C6 prevents relay chatter at lower frequencies.

To check the circuit: (1) Apply an adjustable ac voltage at 1000 Hz to the ac input terminals. (2) Increase the voltage to the point at which relay RY just closes. (3) At this point, read the ac input voltage and, if an ac microammeter is available, the ac input current. (4) Detune the voltage source above and below 1000 Hz, and note

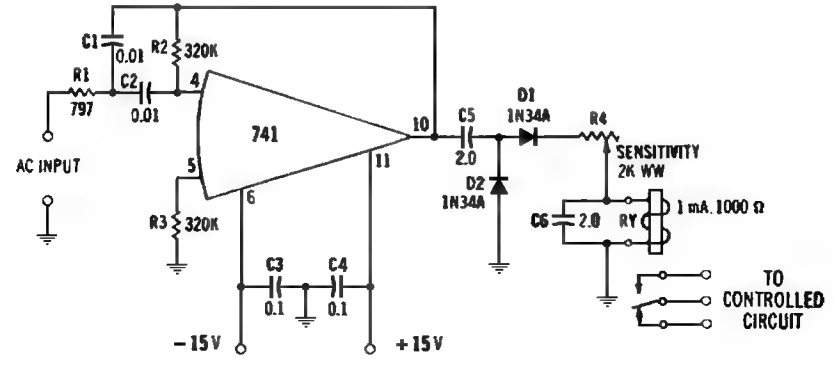


Fig. 3-34. Tuned ac relay.

the higher frequency and lower frequency at which the relay opens (these frequencies mark the bandwidth of the relay circuit). (5) Check the dc drain at (a) zero-signal input and (b) the signal level required for relay closure.

3.35 PHOTORELAY

A light-controlled relay circuit is shown in Fig. 3-35. In this arrangement, the IC, acting as a simple gain-of-10 dc amplifier, steps up the dc output of a self-generating silicon photocell, PC (International S1M-C or equivalent). The amplified output of the IC then drives relay RY, a 1-mA, 1000-ohm unit (Sigma 5F or equivalent). This arrangement permits relay closure at low light intensity. Diode

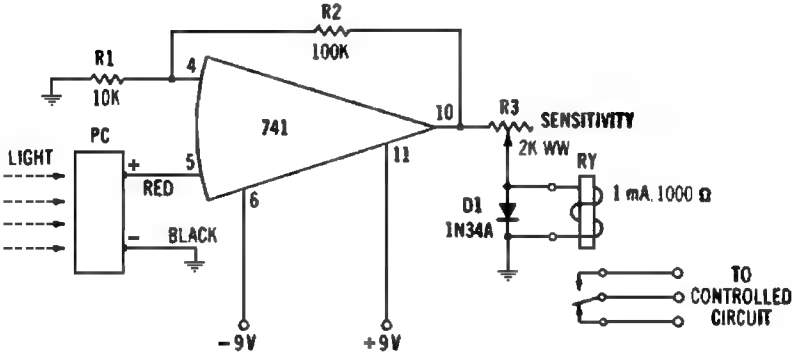


Fig. 3-35. Photorelay.

D1 protects the IC from the high-voltage inductive kick resulting from sudden switch-off of the relay. Through proper selection of the output terminals of the relay, this circuit may either open or close an external circuit, as desired, upon application of illumination. The reverse is also true: the external circuit may be either opened or closed, as desired, upon interruption of illumination.

To check the circuit: (1) Illuminate the photocell with light of the desired intensity. (2) Adjust sensitivity control potentiometer R3 to the point at which the relay just closes. Decreasing R3 makes the circuit respond to lower levels of illumination, and vice versa. (3) Interrupt the light beam and observe if the relay opens as it should. (4) If an adjustable light source and a calibrated light meter are available, set the light intensity to various known levels and observe the settings of potentiometer R3 at which the relay closes. (5) Check

the dc drain with (a) the cell darkened and (b) the cell fully illuminated and the relay closed.

3.36 SOUND RELAY

Fig. 3-36 shows the circuit of a sound-operated relay. In this arrangement, a miniature crystal-microphone cartridge (mic), the sound pickup, is coupled to the input of the IC through a HEP 801 or F0010 FET source follower (Q1). The IC acts as a gain-of-100 audio amplifier the output of which is rectified by diode D1. The dc output of the diode drives relay RY, a 1-mA, 1000-ohm unit (Sigma 5F or equivalent). When switch S1 is at position A, the relay is able to open and close rapidly; when S1 is at B, however, the 5000-μF capacitor (C6) charges on relay closure and, after the signal has passed, holds the relay closed until the charge has dissipated in the relay coil (the time constant here is 5 seconds). Through proper selection of the output terminals of the relay, this circuit may either open or close an external circuit, as desired, upon pickup of sound. The reverse is also true: the external circuit may be either opened or closed, as desired, upon interruption of sound.

To check the circuit: (1) With switch S1 at position A, excite the microphone with steady sound. (2) Adjust sensitivity control potentiometer R6 to the point at which the relay just closes. (If a calibrated

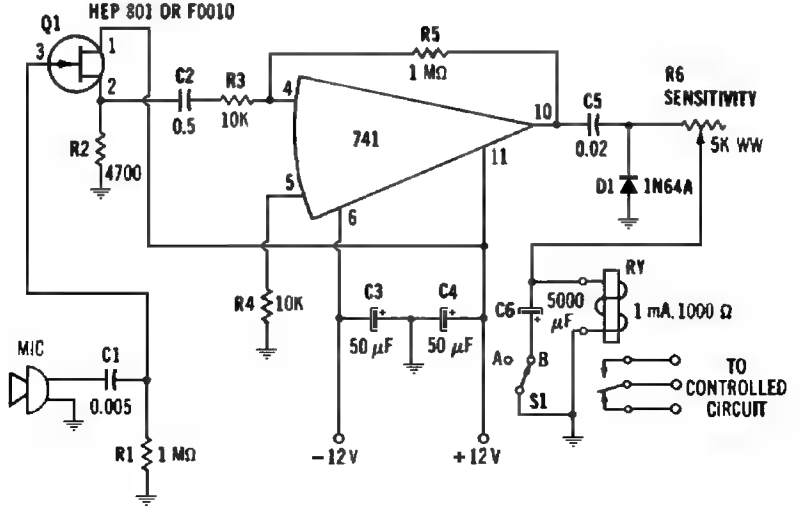


Fig. 3-36. Sound relay.

sound-level meter is available, note the intensity of the sound.) (3) Remove the sound, and observe if the relay drops out as it should. (4) Set switch S1 to position B. (5) Excite the microphone with steady sound, as before in Step 1, to close the relay. (6) Interrupt the sound, noting that the relay holds in for an interval before dropping out. (7) Check the dc drain at (a) zero sound input and (b) maximum sound input.

3..37 PROXIMITY RELAY

The circuit of a simple proximity (capacitance) relay is shown in Fig. 3-37. A finger or body brought close to the small metal pickup plate or disc (maximum diameter 6 inches) couples enough stray pickup into the IC (operated as a gain-of-1000 dc amplifier) to close relay RY in the output of the amplifier. The relay is a 1-mA, 1000-ohm unit (Sigma 5F or equivalent). In the relay section, diode D1 protects the IC from the high-voltage inductive kick resulting from sudden switch-off of the relay. Through proper selection of the output terminals of the relay, this circuit may either open or close an external circuit, as desired, upon approach to the pickup plate. The reverse is also true: the external circuit may be either opened or closed, as desired, upon departure from the plate.

To check the circuit: (1) Have a helper hold the palm of his hand steadily about 1 inch from the pickup plate. (2) Adjust sensitivity control potentiometer R3 to the point at which the relay just closes. (3) Have the helper withdraw his hand, and observe if the relay opens

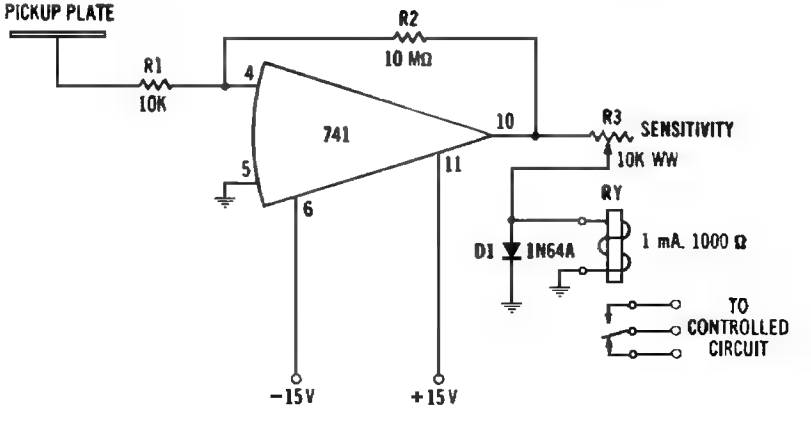


Fig. 3-37. Proximity relay.

readily as it should. (4) Set R3 for maximum sensitivity (minimum resistance) and note how far the hand can be held from the plate and still operate the relay. (5) Check the dc drain when (a) the relay is resting and (b) the relay is closed by capacitance pickup.

3.38 INTERVAL TIMER

Fig. 3-38 shows the circuit of a capacitance-discharge type of interval timer. The range of this device is from less than 1 second to approximately 100 seconds, depending upon the setting of timing potentiometer R1. The circuit operates in the following manner: Push-

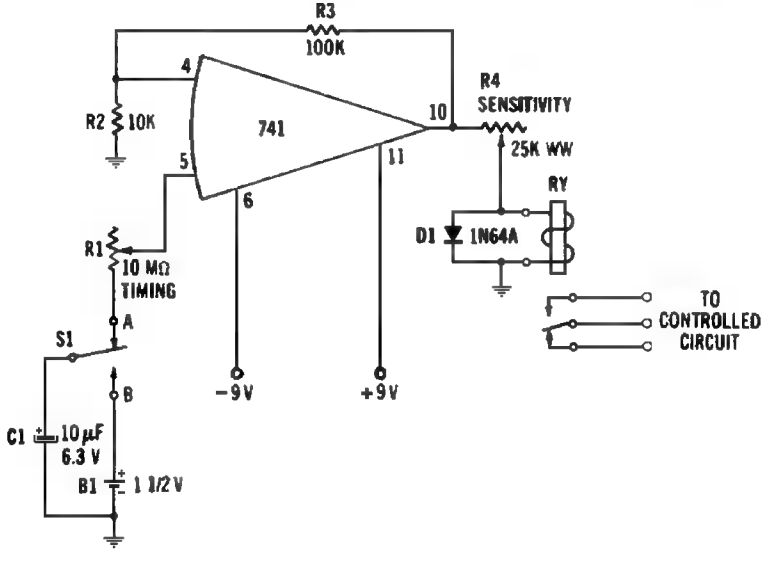


Fig. 3-38. Interval timer.

button switch S1 is normally at position A. When S1 is depressed momentarily and then released, the 10-μF capacitor, C1, charges from 1½-V cell B1 and then discharges through potentiometer R1 and the noninverting input circuit of the IC. The time interval taken to discharge is R1C1 seconds, where R1 is the setting of the timing potentiometer (ohms) and C1 is the capacitance of capacitor C1 (farads). The IC acts as a simple gain-of-10 dc amplifier. The charged capacitor supplies the dc input signal to the IC, and the dc output of the IC actuates relay RY, a 1-mA, 1000-ohm unit (Sigma 5F or equivalent). The relay accordingly remains closed during the

interval taken by capacitor C1 to discharge to a level at which the IC output falls to the dropout voltage of the relay.

The sensitivity control potentiometer, R4, allows the relay to be set for reliable pickup when the voltage across capacitor C1 is at the fully charged value. Diode D1 protects the IC from the high-voltage inductive kick resulting from sudden switch-off of the relay. Through proper selection of the output terminals of the relay, this circuit may either open or close an external circuit, as desired, during the timing interval.

To check the circuit: (1) Set potentiometer R1 arbitrarily or to a point corresponding to a calculated timing interval. (2) Momentarily depress and then release push-button switch S1. (3) Quickly set potentiometer R4 to the point at which the relay closes. (If the relay closes at the existing position of R4, this step will not be required. Once R4 is set, it will not need readjustment.) (4) Repeat Steps 1 and 2, and time the interval between closure and subsequent opening of the relay. (5) By means of repeated Steps 1, 2, and 4, calibrate—directly in seconds—a dial attached to timing potentiometer R1. (6) Check the dc drain (a) with the circuit resting and (b) with the relay closing.

3.39 WAVE SQUARER

The simple arrangement shown in Fig. 3-39 receives a sine-wave input and delivers a square-wave output. Here, a 1N475 zener diode (D1) is inserted into the negative-feedback loop of the IC. The output is clamped at 8 V, the breakdown voltage of the diode, and

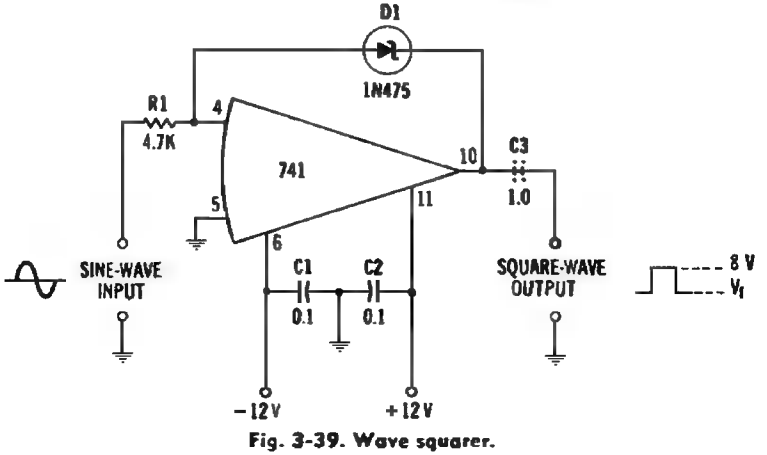


Fig. 3-39. Wave squarer.

swings between that voltage and V_z, the forward voltage of the diode (this excursion is shown in the output-voltage waveform in Fig. 3-39). Output capacitor C3 is required only when strict ac coupling is desired.

To check the circuit: (1) Apply an adjustable-voltage sine-wave signal to the sine-wave input terminals. (2) Observe the waveform of the output signal and check for squareness. (3) Vary the voltage of the input signal and note the value at which the output signal starts squaring. (4) Holding the input-signal voltage constant, vary the frequency and observe the effect upon (a) output squareness and (b) output amplitude. (5) Check the dc drain with (a) zero input signal and (b) maximum input signal.

3.40 LIGHT-BEAM RECEIVER

Fig. 3-40 shows the circuit of a simple receiver for modulated-light-beam communications. The beam impinges upon a self-generating silicon photocell, PC (International S1M-C or equivalent), and

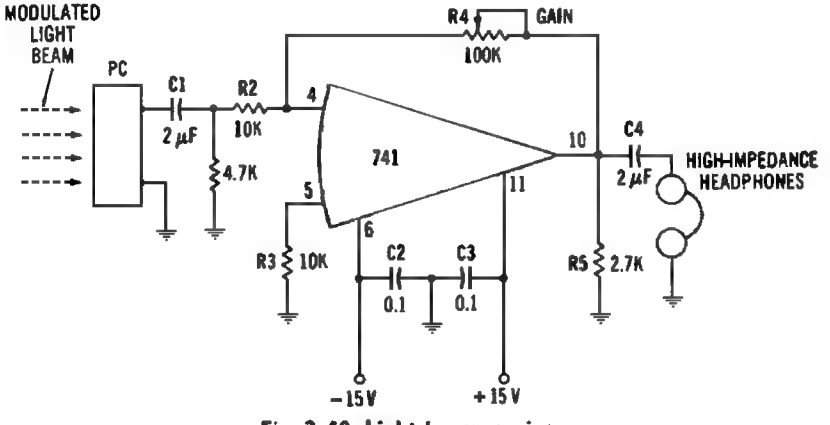


Fig. 3-40. Light-beam receiver.

the corresponding fluctuating output of this cell develops an af voltage across 4.7K resistor R1. The audio voltage is amplified by the IC, and the IC output drives the high-impedance headphones (in lieu of headphones, a power amplifier and loudspeaker may be connected through output capacitor C4). Headphone volume is controlled by adjusting potentiometer R4, which regulates the negative feedback and accordingly the amplifier gain.

To check the circuit: (1) Shine a continuously modulated light beam on photocell PC. (2) Check the corresponding output signal by (a) listening with headphones and (b) measuring the af voltage across the headphones. (3) Repeat Steps 1 and 2 at selected settings of gain control potentiometer R4, noting the effect of the setting on the output-signal volume. (4) With potentiometer R4 set at a chosen point, repeat Steps 1 and 2 at different modulation frequencies, while observing the output-signal voltage at each frequency. (5) Check the dc drain at (a) zero-signal input and (b) maximum-signal input.

3.41 PHASE REVERSER

Fig. 3-41 shows the circuit of a single-ended, common-ground phase reverser. When phase switch S1 is at position A, the output-signal phase is zero (or a selected reference value); when S1 is at B, the output-signal phase is 180° different. This arrangement utilizes the phase reversal of the inverting section (terminal 4) of the 741 IC. With the switch at position A, the input signal is sampled, whereas when S1 is at B, the IC output is sampled. The amplitude of the output may be adjusted, by means of potentiometer R3, to equal the input or to exceed it, as required in a particular application of the shifter.

To check the circuit: (1) With switch S1 thrown to position A, apply a 1000-Hz sine-wave signal to the ac input terminals. (2) Observe the phase of the output signal by means of an oscilloscope or phase meter connected to the ac output terminals. (3) Throw S1 to

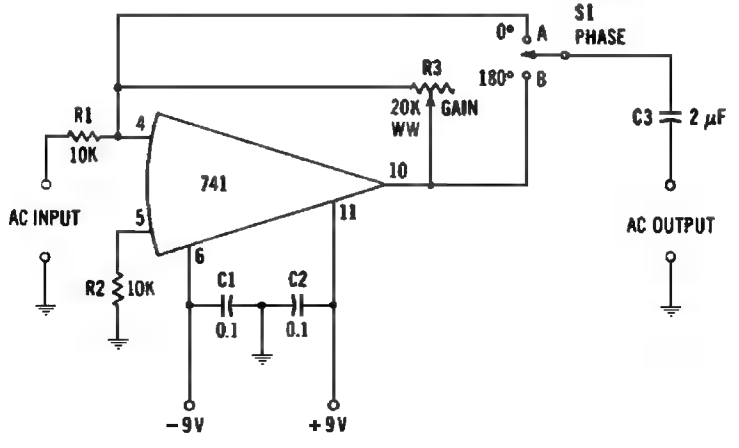


Fig. 3-41. Phase reverser.

position B, and observe the phase of the output signal, which should appear rotated 180°. Adjust potentiometer R3 for an amplitude suitable for observation. (4) Repeat Steps 1 through 3 at various frequencies, noting the effect of frequency on phase reversal and on amplitude. (5) Check the dc drain at (a) zero-signal input and (b) maximum-signal input.

Index

A

Ac
  follower operation, 56-58
    inverting type, 58
    noninverting type, 56-57
  input-voltage range, 52-53
  output-voltage swing, maximum, 50-51
  relay, tuned, 99-100
  test signal, 28
  voltage gain
    closed-loop, 43-44
    open-loop, 42-43
Adder, analog, 86-87
Af/rf relay, sensitive, 98-99
Amplifier
  audio
    gain-of-
      10, 70-71
      100, 71-72
      1000, 72
    single-supply, 74
  dc, 76
  differential, 17-18
  limiter, 73-74
  noninverting, 73
  operational, 19-21
  voltage-follower, 70
Analog
  adder, 86-87
  -type audio frequency meter, 94-95
Astable multivibrator, 79
Audio
  amplifier
    gain-of-
      10, 70-71
      100, 71-72
      1000, 72
    single-supply, 74
  frequency meter, analog-type, 94-95
  mixer, 75-76
  oscillator
    twin-T, 76-77
    Wien-bridge, 78

B

Bandpass filter, 81-82, 82-83

C

Capacitors, 29
  IC, 13-14
Closed-loop
  ac voltage gain, 43-44
  dc voltage gain, 39-41
  frequency response, 46-47
Common-mode
  gain, 18
  operation, 18
  rejection, 18, 54-55
Constant-current sink, [illegible]
Converter, logarithmic, 91-92

Current
gain, 63-64
offset, input, 38-39
operating, 30-31

D

Dc
amplifier, 76
follower operation, 55-56
input-voltage range, 51-52
microammeter, electronic, 88-89
millivoltmeter, electronic, 89-90
operating voltages, 29-30
output-voltage swing, maximum, 48-50
relay, sensitive, 97-98
supply, 27-28
test signal, 28
voltage gain, closed-loop, 39-41
voltmeter, electronic, 90-91
Differential amplifier, 17-18
Differentiator, 84
Digital ICs, 12
Diode, IC, 12
DIP package, 15
Dual-in-line package, 15

E

Electronic
dc
microammeter, 88-89
millivoltmeter, 89-90
voltmeter, 90-91
thermometer, 93-94
Electroscope, 96-97
Experiments, nature of, 23-24

F

Field(s), 22
-effect transistors, 19
Filter
bandpass, 81-82, 82-83
high-pass, 80-81
low-pass, 79-80
notch, high-Q, 83-84
Flat pack, 15
Follower
ac, operation, 56-58
inverting type, 58
noninverting type, 56-57
dc, operation, 55-56
voltage-, amplifier, 70

Frequency
meter, audio, analog-type, 94-95
response
closed-loop, 46-47
open-loop, 44-46
unity-gain, 47-48

G

Gain
common-mode, 18
current, 63-64
voltage
ac
closed-loop, 43-44
open-loop, 42-43
dc, closed-loop, 39-41
Generators, signal, 28

H

High-
pass filter, 80-81
Q notch filter, 83-84

IC, 11
capacitors in, 13-14
digital, 12
diode in, 12
linear, 12
packages, 15
precautions in handling, 21-22
resistor in, 13
symbols, 16-17
transistors in, 12-13
Type 741, 22
unit, as a, 15
used in this book, 22
Impedance
input, 58-60
output, 60-62
Input
impedance, 58-60
inverting, 19-20
noninverting, 19-20
offset
current, 38-39
voltage, 37-38
/output isolation, 22
protection, 21
resistance, milliammeter with low, 87-88

Input—cont
voltage
ac, range of, 52-53
dc, range of, 51-52
Installation, 21
Instrument switching, 28
Integrated circuit, 27
economics of, 21
nature of, 11-15
Integrator, 84-85
Interval timer, 103-104
Inverting input, 19-20
Isolation, input/output, 22

J

JFETs, 19

L

Labeling, terminal, 27
Leads, 28
Light
-beam receiver, 105-106
meter, sensitive, 92-93
Limiter amplifier, 73-74
Linear ICs, 12
Logarithmic converter, 91-92
Low-pass filter, 79-80

M

Mechanical shock, 21
Meter(s), 28
frequency, audio, analog-type, 94-95
light, sensitive, 92-93
sound-level, 95-96
Microammeter, dc, electronic, 88-89
Milliammeter, low input resistance, with, 87-88
Millivoltmeter, dc, electronic, 89-90
Mini-DIP package, 15
Mixer, audio, 75-76
MOSFETs, 19
Multivibrator, astable, 79

N

Noninverting
amplifier, 73
input, 19-20
Notch filter, high-Q, 83-84
Null, offset, adjustment, 34-37
external, 37
internal, 36-37

O

Offset
current, input, 38-39
null adjustment, 34-37
external, 37
internal, 36-37
voltage
input, 37-38
output, 31-32
Op amps, 19
Open-loop
ac voltage gain, 42-43
frequency response, 44-46
Operating
current, 30-31
voltages, dc, 29-30
Operational amplifier, 19-21
Oscillator, audio
twin-T, 76-77
Wien-bridge, 78
Oscilloscope, 28
Output
impedance, 60-62
offset voltage, 31-32
polarity, 32-34
voltage
ac, swing, maximum, 50-51
dc, swing, maximum, 48-50

P

Package
DIP, 15
dual-in-line, 15
flat pack, 15
IC, 15
mini-DIP, 15
Phase reverser, 106-107
Photorelay, 100-101
Polarity
output, 32-34
power-supply, 22
Potentiometers, 29
Power-supply
polarity, 22
rejection ratio, 64-66
Precautions in handling ICs, 21-22
Precision rectifier, 85-86
Procedure, step-by-step, 27

Protection, input, 21
Proximity relay, 102-103

R

Ratings, maximum, 22
Receiver, light-beam, 105-106
Rectifier, precision, 85-86
Rejection
  common-mode, 18, 54-55
  ratio, power-supply, 64-66
Relay
  ac, tuned, 99-100
  af/rf, sensitive, 98-99
  dc, sensitive, 97-98
  proximity, 102-103
  sound, 101-102
Resistance, input, milliammeter with low, 87-88
Resistors, 28
  IC, 13
Reverser, phase, 106-107

S

Sequence, 27
  in energizing, 22
741 IC, 22
Shock, mechanical, 21
Signal
  generators, 28
  test
    ac, 28
    dc, 28
Single-supply audio amplifier, 74
Sink, constant current, 18
Slew rate, 62-63
Soldering, 21
Sound
  -level meter, 95-96
  relay, 101-102
Squarer, wave, 104-105
Supply, dc, 27-28
Switching, instrument, 28
Symbols, IC, 16-17

T

Temperature, 22
Terminal labeling, 27
Test signal
  ac, 28
  dc, 28
Thermometer, electronic, 93-94
Timer, interval, 103-104
Transistors
  field effect, 19
  IC, 12-13
Tuned ac relay, 99-100
Twin-T audio oscillator, 76-77

U

Unity-gain frequency, 47-48

V

Voltage
  -follower amplifier, 70
  gain
    ac,
      closed-loop, 43-44
      open-loop, 42-43
    dc, closed-loop, 39-41
  input
    ac, range of, 52-53
    dc, range of, 51-52
  offset
    input, 37-38
    output, 31-32
  operating, dc, 29-30
  output
    ac, swing, maximum, 50-51
    dc, swing, maximum, 48-50
Voltmeter, dc, electronic, 90-91

W

Wave squarer, 104-105
Wien-bridge audio oscillator, 78

1 electronic ac voltmeter (M1)—*optional*
2 0.1-μF capacitors (C1, C2)
1 1.0-μF capacitor (C3)
1 10K resistor (R1)
1 100K resistor (R2)
1 1K wirewound potentiometer (R3)
1 dpst switch (S1-S2)
1 spst switch (S3)
1 +15 V dc supply (V_{CC})
1 −15 V dc supply (V_{EE})

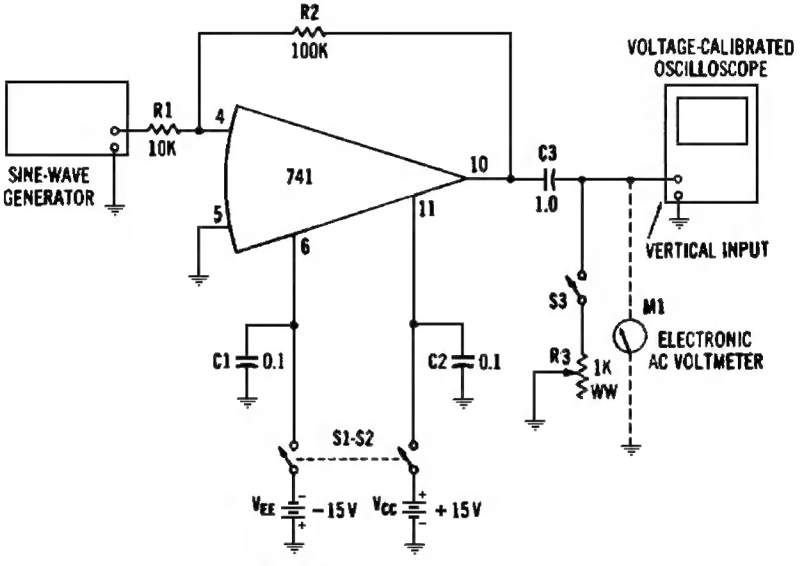


Fig. 2-27. Output impedance

Test Procedure

1. With switches S1-S2 and S3 open, potentiometer R3 set to maximum resistance, the oscilloscope and generator off, and the generator output attenuator set to zero, set up the test circuit as shown in Fig. 2-27.
2. Set the generator to 1000 Hz.
3. Close switch S1-S2, switch on the generator, and switch on the oscilloscope.
4. Adjust the generator output attenuator for maximum undistorted signal, as indicated by the oscilloscope. Read the value of IC output-signal voltage (V_o) from the oscilloscope or from meter M1.